JVC

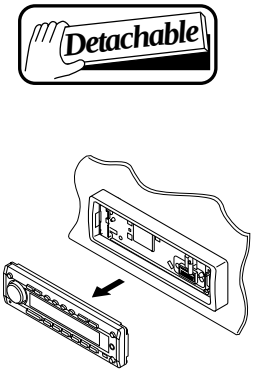
SERVICE MANUAL

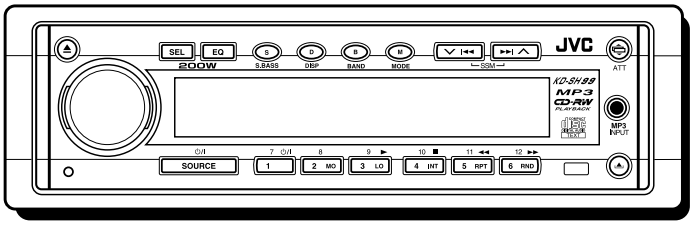
CD RECEIVER

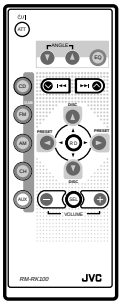
KD-SH99

Area Suffix

J ------ Northern America







COMPACT disc DIGITAL AUDIO TEXT

CD-RW PLAYBACK

MP3

Contents

No.49643
Jun. 2001

Safety precaution

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

⚠ ***CAUTION*** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

Preventing static electricity

1.Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2.About the earth processing for the destruction prevention by static electricity

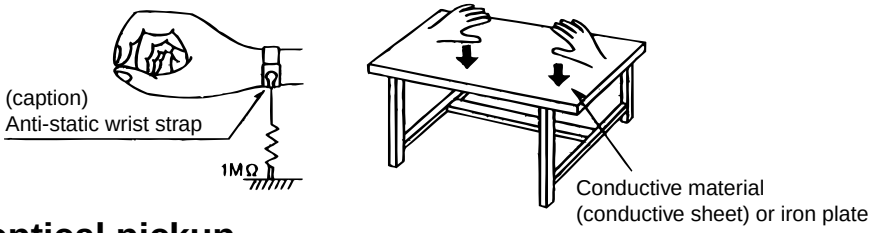
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players.
Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

4.Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

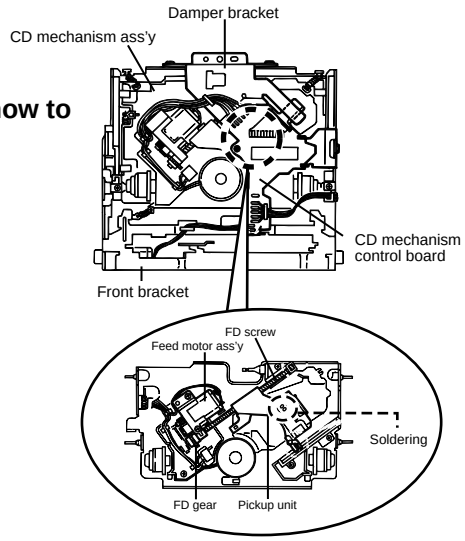
3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Attention when traverse unit is decomposed

***Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.**

1.Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure.
(When the wire is removed without putting up solder, the CD pick-up assembly might destroy.)
2.Please remove solder after connecting the card wire with when you install picking up in the substrate.



Disassembly method

■ Removing the front panel assembly

(See Fig.1)

1. Press the release button in the lower right part of the front panel assembly to unlock.

2. Remove the front panel assembly in the direction of the arrow.

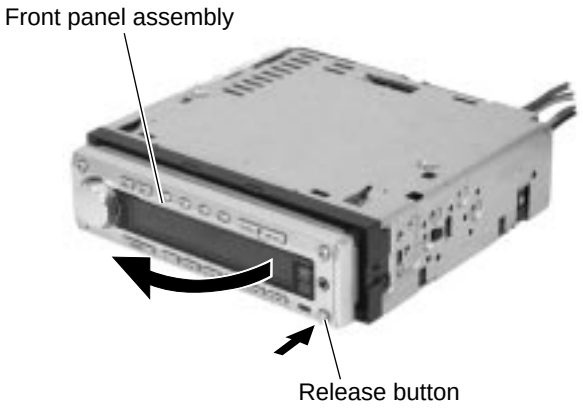


Fig.1

■ Removing the top chassis

(See Fig.2 to 6)

- Turn on power.

1. Press the eject button in the upper left part of the front panel assembly to move the assembly as shown in Fig.2 and turn off power.

2. Remove the two screws **A** on the upper side of the body.

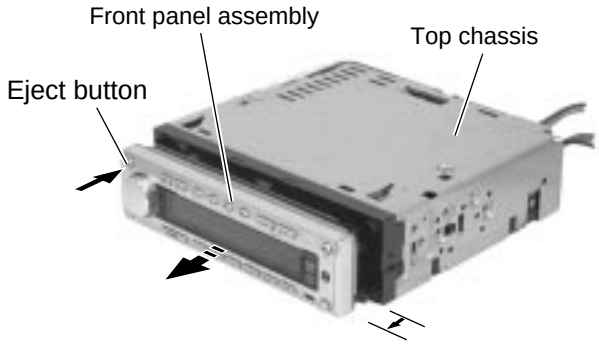


Fig.2

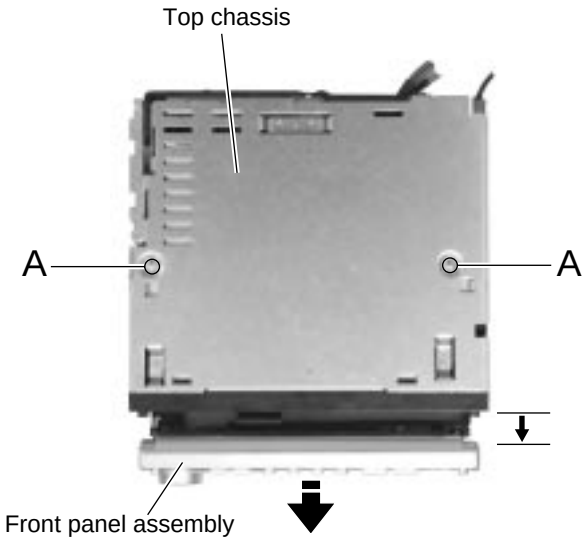


Fig.3

3. Remove the three screws **B** on both sides of the body.

4. Remove the screw **C** and the three screws **D** on the left side of the body.

5. Remove the two screws **E** and the screw **F** on the back of the body.

6. Move the top chassis upward and remove it with the CD mechanism assembly. The connector on the CD mechanism assembly is disconnected from connector CN601 on the main board.

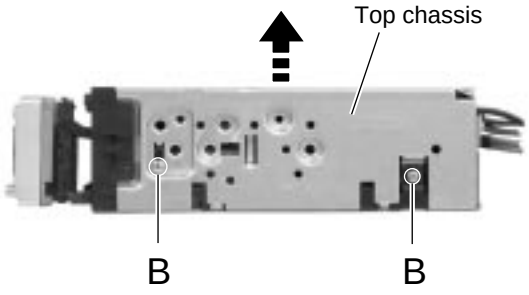


Fig.4

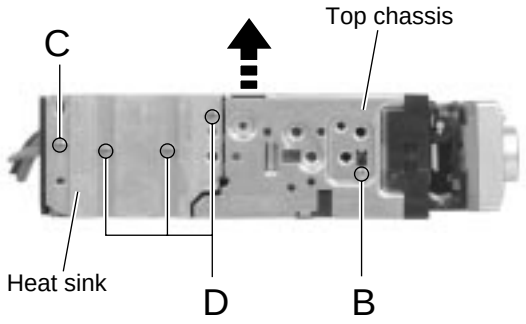


Fig.5

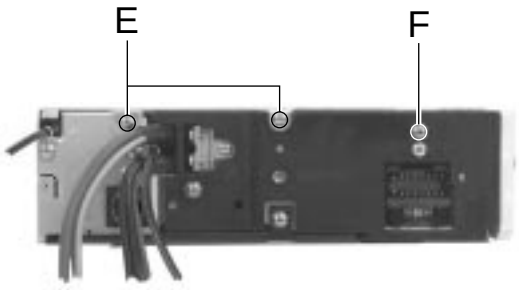


Fig.6

■ Removing the CD mechanism assembly (See Fig.7)

- Prior to performing the following procedure, remove the top chassis.

1. Remove the three screws **G** inside the top chassis and remove the CD mechanisma ssembly.

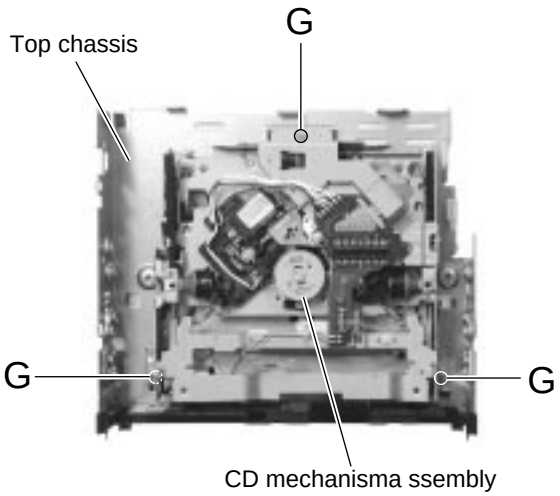


Fig.7

■ Removing the motor assembly (See Fig.8 to 10)

- Prior to performing the following procedure, remove the top chassis.

1. Disconnect the wire from connector CN703 on the main board.
2. Remove the motor bracket and the spring attached to the arm braket assembly (R).
3. Remove the two screws **H** attaching the motor bracket.
4. Remove the washer attaching the clutch assembly and pull out the clutch assembly from the shaft.
5. Remove the two screws **I** and the motor assembly from the motor bracket.

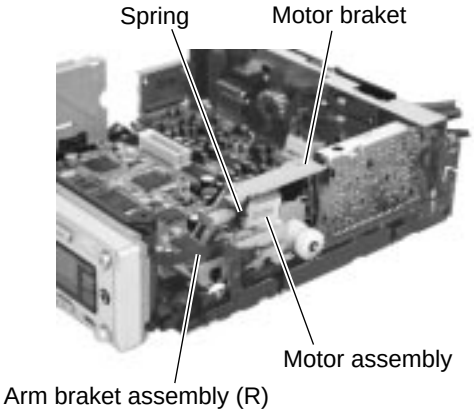


Fig.8

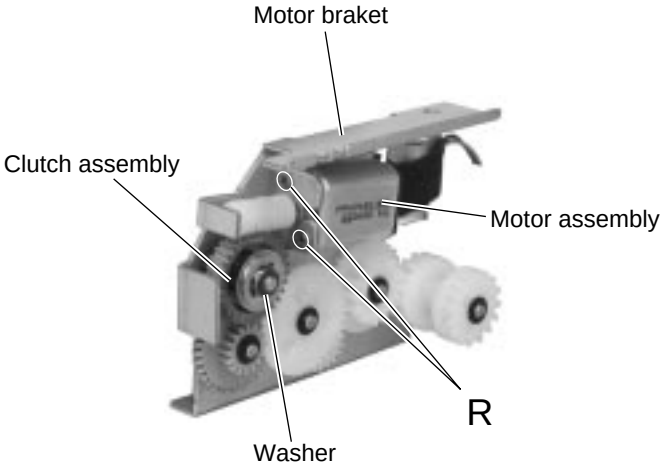


Fig.10

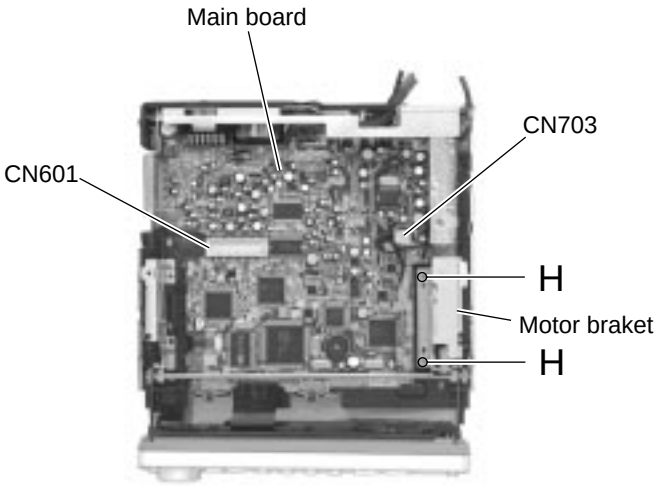


Fig.9

■ Removing the main board

(See Fig.11 to 15)

- Prior to performing the following procedures, remove the top chassis and the motor bracket.

1. Disconnect the flexible wire from connector CN701 and CN702 on the main board respectively.

2. Move the front bracket backward until it stops.

3. Remove the four screws **J** attaching the arm brackets (L) and (R). Move the right and arm lefter brackets from the rod gear.

4. Remove the rod gear.

5. Remove the screw **K** attaching the rear panel to the bottom cover on the back of the body.

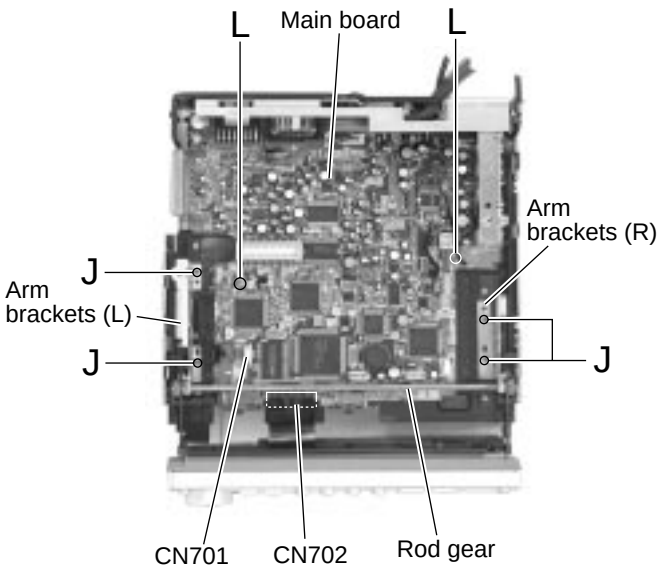


Fig.11

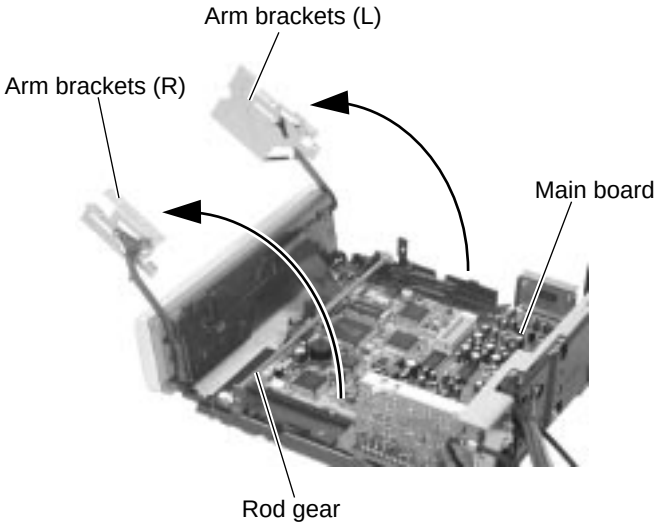


Fig.12

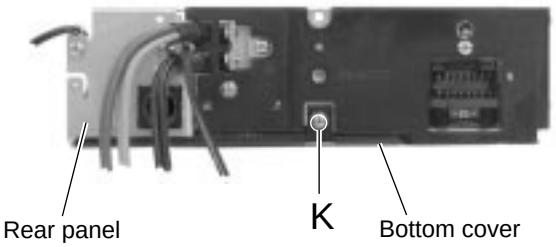


Fig.13

6. Remove the two screws **L** and move the main board backwards to release the two joints **a**. (The main board will be removed with the rear panel and the rear heat sink)

7. Remove the screw **M** and **N** attaching the rear heat sink.

8. Remove the three screws **O** and the screw **P** attaching the rear panel. Remove the main board.

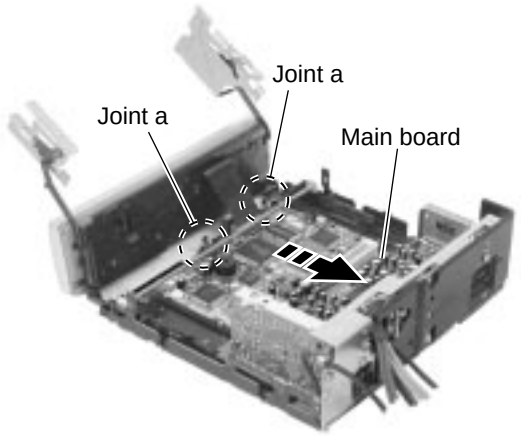


Fig.14

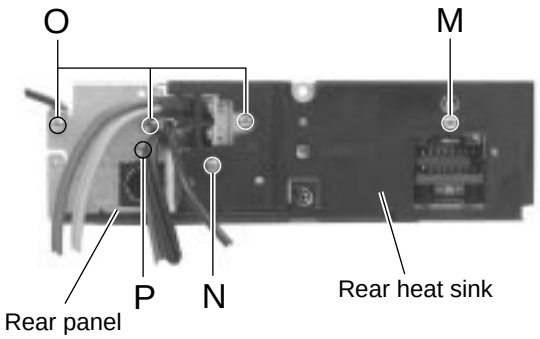


Fig.15

■ Removing the lifter switch board (See Fig.16)

- Prior to performing the following procedures, remove the top chassis, the motor bracket and the main board.

1. Remove the two screws **Q** attaching the lifter switch board.

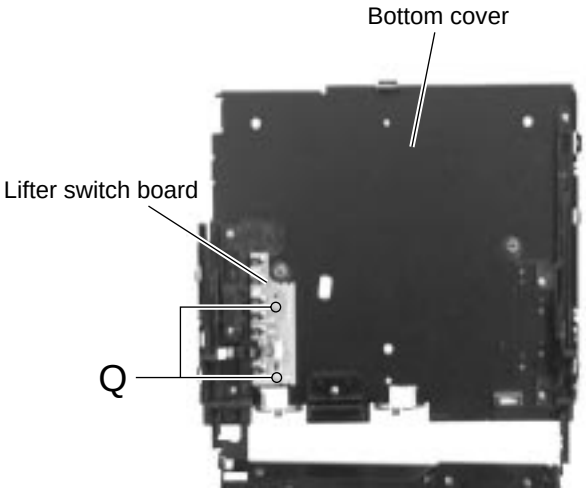


Fig.16

■ Removing the lifter board

(See Fig.17 to 23)

- Prior to performing the following procedure, remove the top chassis assembly and thefront panel assembly.

1. Disconnect the flexible wire from connector CN702 on the main board.

2. Remove the four screws **R** attaching the front bracket on both sides of the body.

3. Push the pin of the joint **c** on the front of the front bracket to release the lock lever.

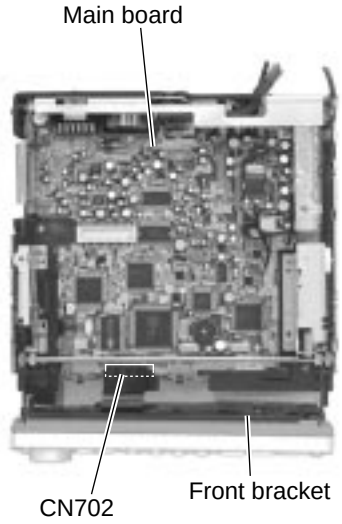


Fig.17

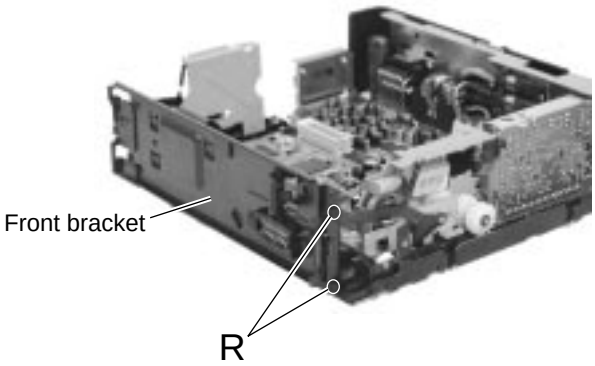


Fig.18

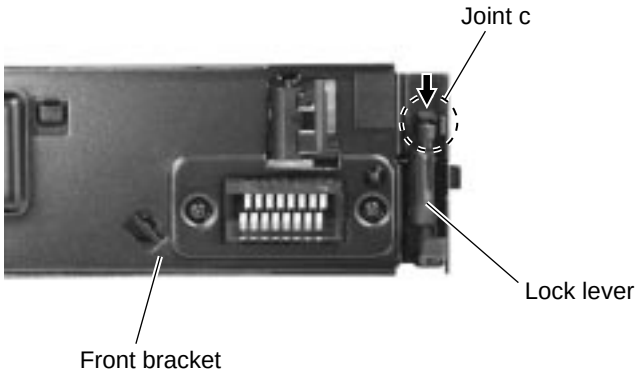


Fig.20

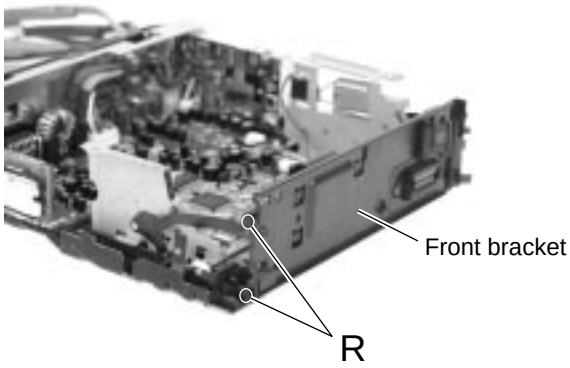


Fig.19

4. Remove the screw **S** attaching the lifter board cover in the rear of the front bracket.

5. Release the two joints **d** while pushing the front side. Move the lifter board cover inthe direction of the arrow and release the eight joints **e**.

6. Remove the two screws **T** attaching the lifter board on the front of the body.

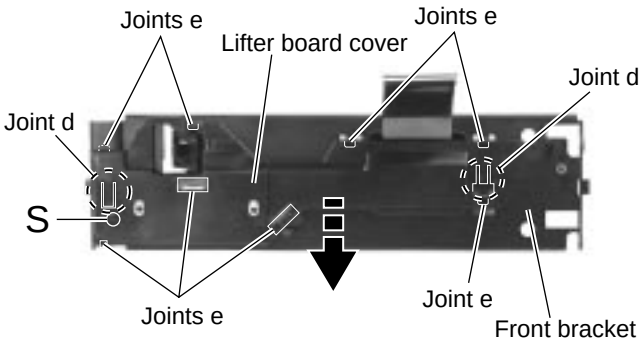


Fig.21

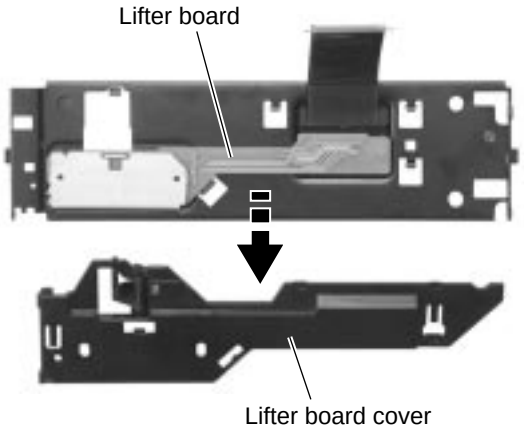


Fig.22

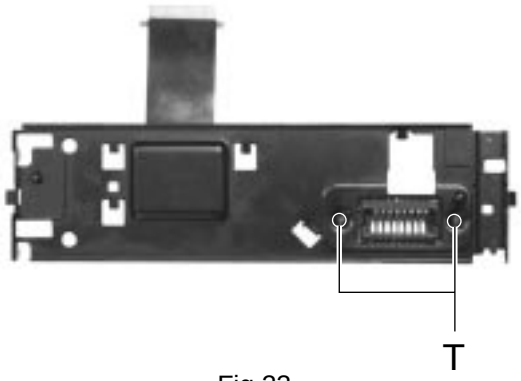


Fig.23

<Front panel assembly>

・ Prior to performing the following procedure, remove the front panel assembly.

■Removing the front board
(See Fig.24 and 25)

1. Remove the four screws **U** attaching the rear panel to the front panel assembly.
2. Release the eleven joints **f** of the front panel and the rear panel.
3. Disconnect the wire from connector CN503 on the front board.
4. If necessary, unsolder connector CN502 on the front board.

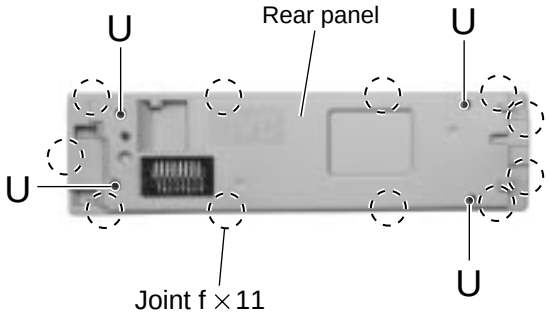


Fig.24

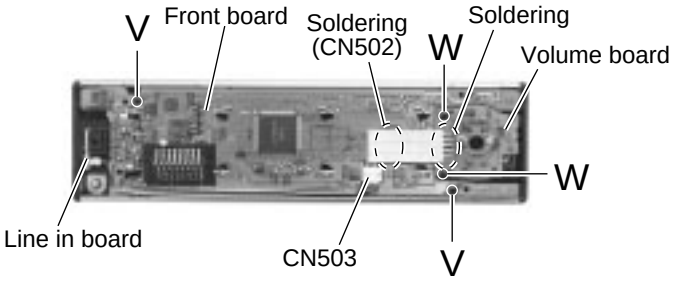


Fig.25

■Removing the volume board
(See Fig.25 and 26)

・ Prior to performing the following procedure, remove the rear panel.

1. Remove the two screws **W** attaching the volume board.
2. Disconnect the volume knob, ring lens and volume ring from the volume board.
3. If necessary, unsolder the volume board.

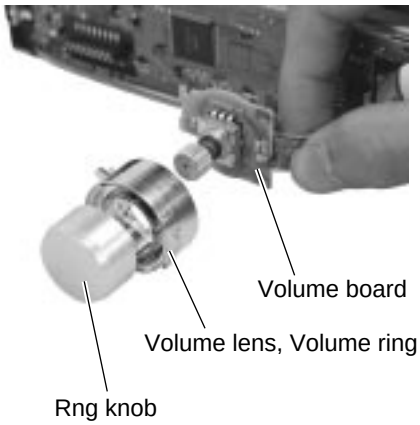


Fig.26

■Removing the line in board
(See Fig.25 and 27)

・ Prior to performing the following procedure, remove the rear panel.

1. Disconnect the wire from connector CN503 on the front board.
2. Pull out the line in board from the front panel assembly.

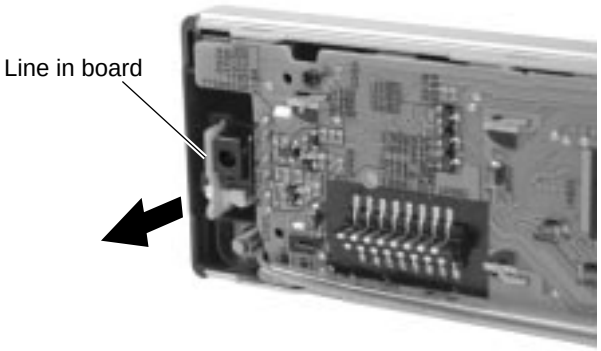


Fig.25

<CD mechanism section>

■Removing the CD mechanism control board (See Fig.1 and 2)

1. Unsolder the part **a** and **b** on the CD mechanism control board.
2. Remove the stator fixing the CD mechanism control board and the damper bracket (To remove the stator smoothly, pick up the center part).
3. Remove the screw **A** attaching the CD mechanism control board.
4. Remove the CD mechanism control board in the direction of the arrow while releasing it from the two damper bracket slots **d** and the front bracket slot **e**.
5. Disconnect the flexible wire from connector on the pickup unit.

ATTENTION: Turn the FD gear in the direction of the arrow to move the entire pickup unit to the appropriate position where the flexible wire of the CD mechanism unit can be disconnected easily.
(Refer to Fig.2)

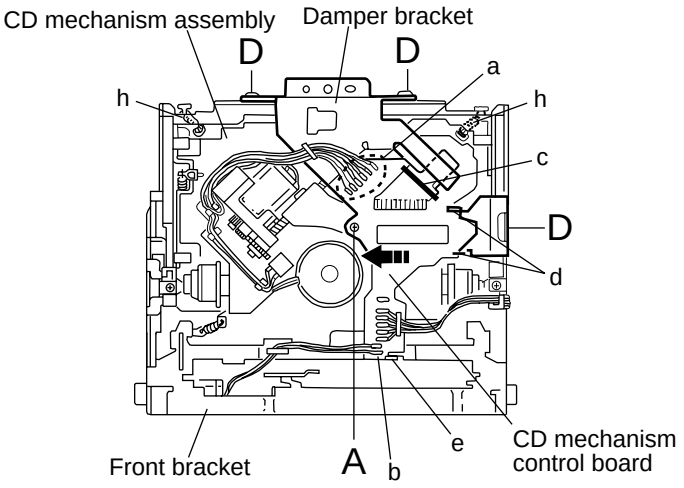


Fig.1

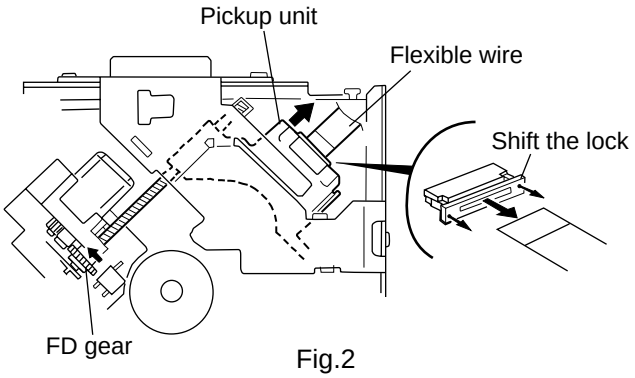


Fig.2

■Removing the loading motor (See Fig.3 to 5)

- Prior to performing the following procedure, remove the CD mechanism control board.

1. Remove the two springs **f** attaching the CD mechanism assembly and the front bracket.
2. Remove the two screws **B** and the front bracket while pulling the flame outward.
3. Remove the belt and the screw **C** from the loading motor.

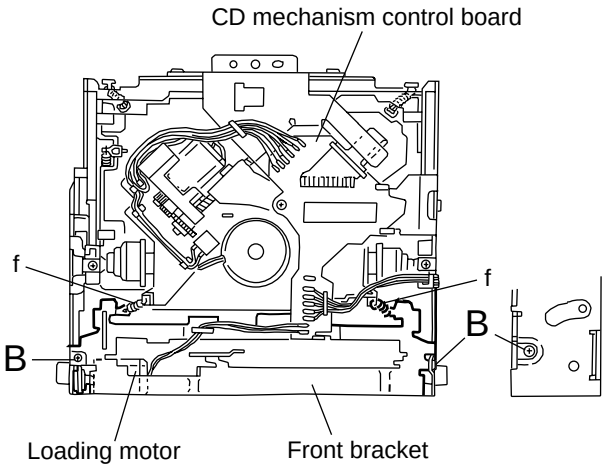


Fig.3

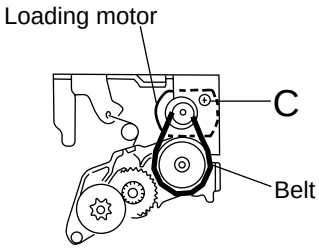


Fig.5

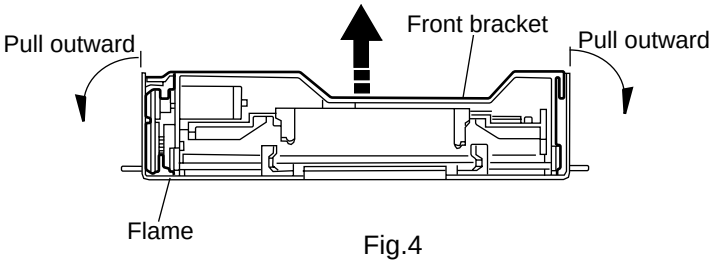


Fig.4

■ Removing the CD mechanism assembly (See Fig.1, 6 to 9)

- Prior to performing the following procedure, remove the CD mechanism control board and the front bracket (loading motor).

1. Remove the three screws **D** and the damper bracket.

2. Raise the both sides fix arms and move the fix plates in the direction of the arrow to place the four shafts **g** as shown in Fig.8 and 9.

3. Remove the CD mechanism assembly and the two springs **h** attaching the flame.

4. Remove the two screws **E** and both sides rear damper brackets from the dampers. Detach the CD mechanism assembly from the left side to the right side.

ATTENTION: The CD mechanism assembly can be removed if only the rear damper bracket on the left side is removed.

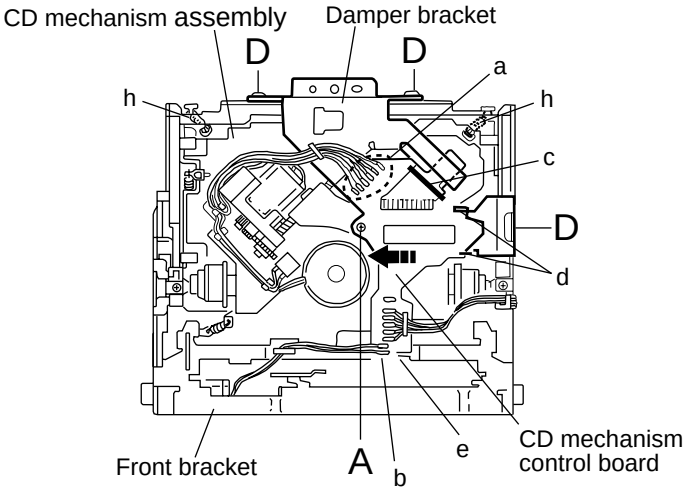


Fig.1

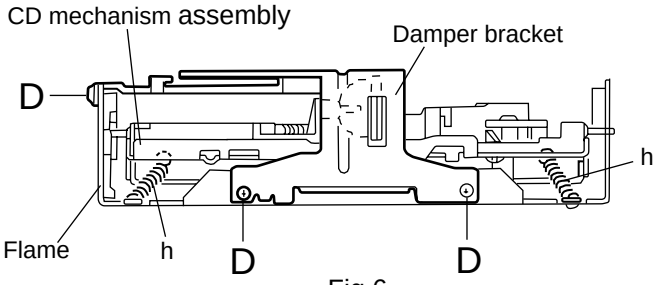


Fig.6

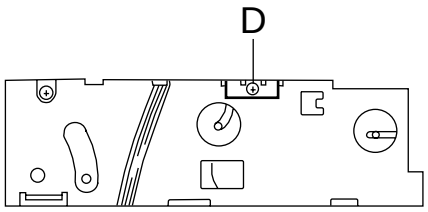


Fig.7

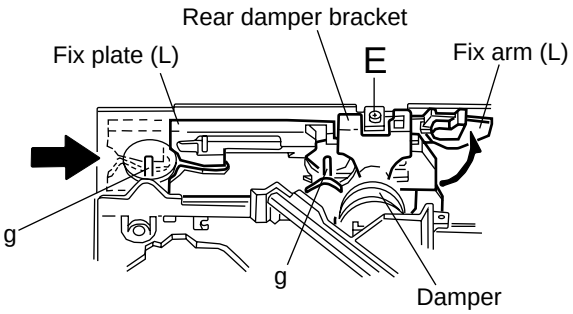


Fig.8

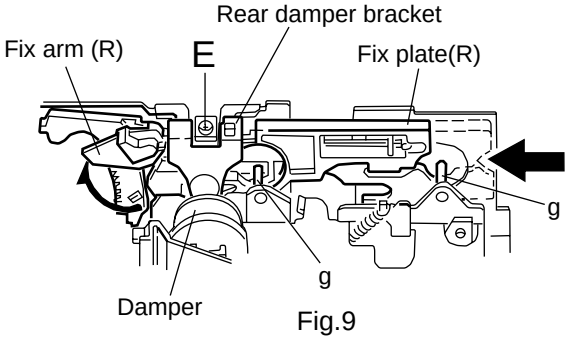


Fig.9

■ Removing the feed motor assembly (See Fig.10)

・ Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor) and the CD mechanism assembly.

1. Remove the two screws **F** and the feed motor assembly.

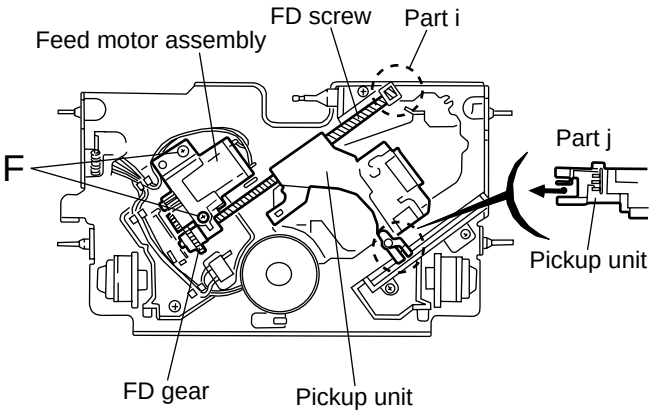


Fig.10

■ Removing the pickup unit (See Fig.10 and 11)

・ Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.

1. Detach the FD gear part of the pickup unit upward. Then remove the pickup unit while pulling out the part **i** of the FD screw.

> ATTENTION: When reattaching the pickup unit, reattach the part **j** of the pickup unit, then the part **i** of the FD screw.

2. Remove the screw **G** attaching the nut push spring plate and the pickup mount nut from the pickup unit. Pull out the FD screw.

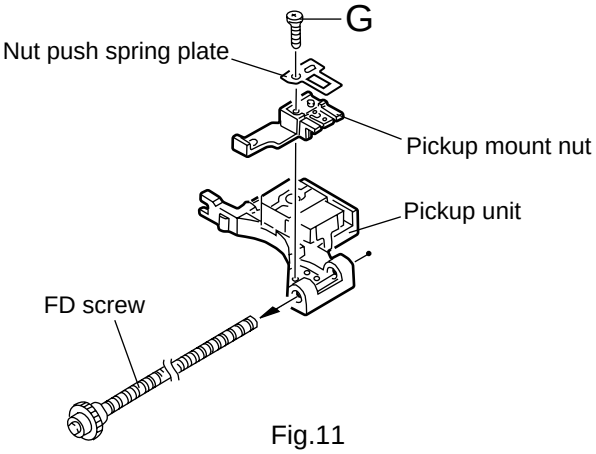


Fig.11

■ Removing the spindle motor (See Fig.12 and 13)

・ Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.

1. Turn up the CD mechanism assembly and remove the two springs **k** on both sides of the clamper arms. Open the clamper arm upward.

2. Turn the turn table, and remove the two screws **H** and the spindle motor.

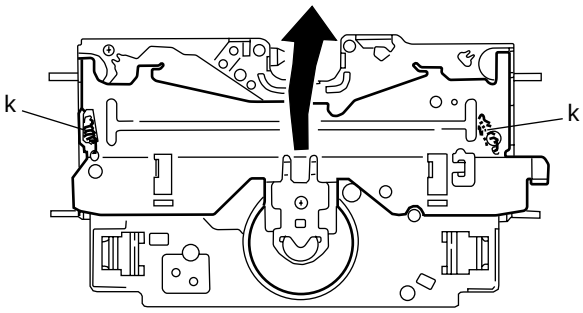


Fig.12

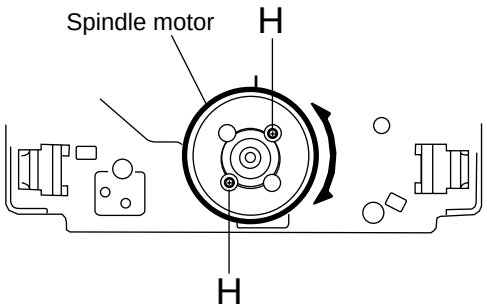


Fig.13

Adjustment method

■ Test instruments required for adjustment
1. Digital oscilloscope (100MHz)
2. AM Standard signal generator
3. FM Standard signal generator
4. Stereo modulator
5. Electric voltmeter
6. Digital tester
7. Tracking offset meter
8. Test Disc JVC :CTS-1000
9. Extension cable for check
EXTGS004-26P×1

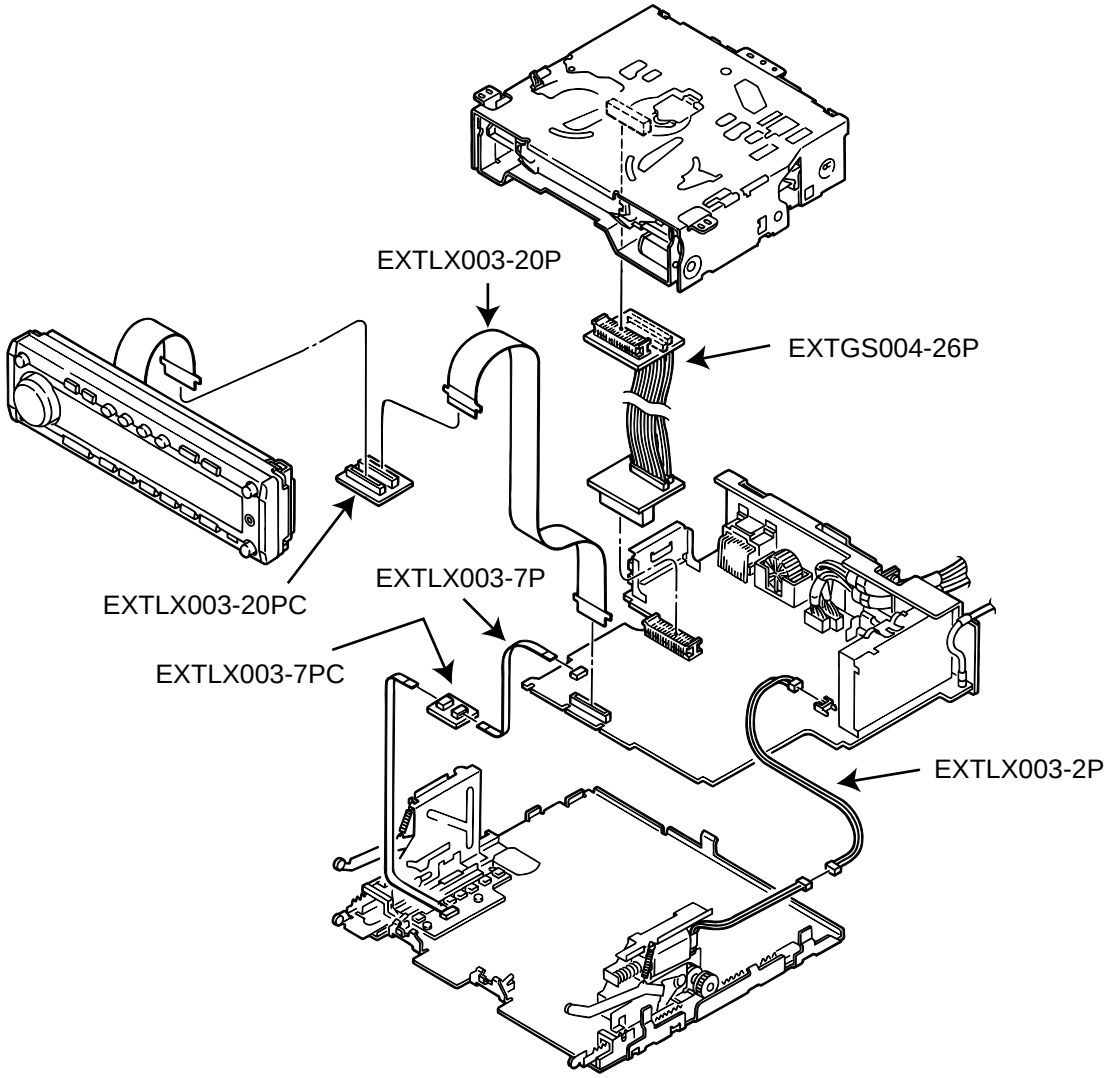
■ Standard volume position
Balance and Bass &Treble volume : Indication"0"
Loudness : OFF
BBE : OFF

■ Frequency Band
FM 87.5MHz ~107.9MHz(with channel interval set to 200kHz)
FM 87.5MHz ~108.0 MHz(with channnel interval set to 50kHz)
AM 530kHz ~ 1710 kHz(with channel interval set to 10kHz)
AM 531 kHz ~ 1602 kHz(with channel interval set to 9 kHz)

■ Dummy load
Exclusive dummy load should be used for AM,and FM. For FM dummy load,there is a loss of 6dB between SSG output and antenna input.The loss of 6dB need not be considered since direct reading of figures are applied in this working standard.

■ Standard measuring conditions
Power supply voltage DC14.4V(11 V to 16V allowance)
Load impedance 4 Ω (4 Ω to 8 Ω allowance)
Line-Out Level/Impedance 4.0V/20kΩload(fuull scall)

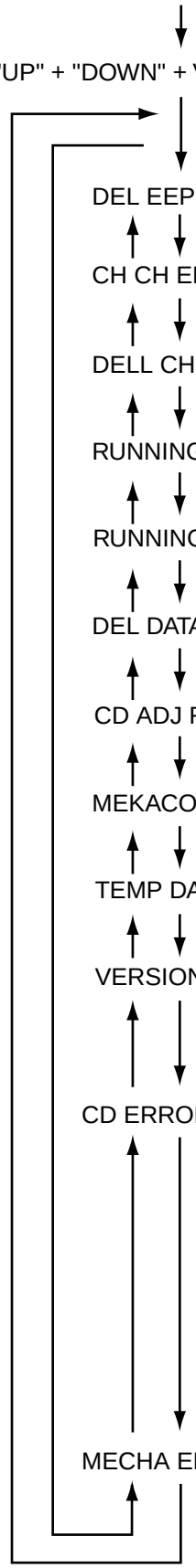
■ How to connect the extension cable for adjusting



< Service mode >

The menu in the service mode can be switched with UP/DOWN.
The menu selected by the SEL button input is executed.

The ordinary mode



"UP" + "DOWN" + VR counterclockwise rotation.

DEL EEPROM — EEPROM data all clear (changer is connected).

CH CH ERR — CD changer error career call (changer is connected).

DELL CH ERR — CD changer EEPROM clear (EEPROM career)

RUNNING CD — CD running mode (Do not use in service).

RUNNING SH — Running mode of front panel (Do not use in service).

DEL DATA — CD ERROR MECHA ERR error career deletion.

CD ADJ R — Self adjustment value call (It is a display switch with VR).

MEKACON WR — Sub-microcomputer writing (Do not use in service).

TEMP DATA — Temperature data call.

VERSION — Microcomputer version confirmation.
The display changes in the up/down key.
The main microcomputer : SH99 J203
The Sub-microcomputer : SH99S 122

CD ERROR — CD relation error career reading

< Error display >

Item	Content
DISC_ERROR_0	Others
DISC_ERROR_1	FOCUS NG
DISC_ERROR_2	Self adjustment NG
DISC_ERROR_3	CLV NG
DISC_ERROR_4	TOC reading NG or MP3 FILE CHECK NG
DISC_ERROR_5	BLANK DISC
EJECT_ERR	

MECHA ERR — Panel relation error career reading

<ERROR CODE of Panel mechanism>

Memory to EEPROM of 6 digits, 1st and 2nd digit are indicate the operation mode when occur the error, 3rd to 6th digit are indicate details of error.
LCD indication time is use lower 2digits of details of error.
This series is indicate **ERR XX** (XX is error code).
<ex.> When details of error is 0A0001 , it is indicate **ERR 01**, details of error is 0E0031 , it is **ERR 31**.
Switch is from this side sequentially PSW1, PSW2,.....PSW6.

Details of error	Error code
1. Error of door open (fault of PSW1)	
(1) Time out by PSW1 not changed	0A0001
(2) PSW1 change during waiting 300ms after open position detected	0A0002
2. Error of door close (fault of PSW6)	
(1) Time out by PSW6 not changed	0B0006
(2) PSW6 change during waiting 300ms after close position detected	0B0007
3. Error of shift to DETACH position (fault of PSW5)	
(1) Time out by PSW5 not changed to open side	0C0011
(2) Shift to open side, pass the DETACH position then detect ANGLE1	0C0012
(3) Time out by PSW5 not changed to close side	0C0013
(4) Shift to close side, pass the DETACH position then detect close position	0C0014
4. Error of angle adjustment 4-1 Shift to ANGLE1 (fault of PSW4)	
(1) Time out by PSW4 not changed to shift for open side	0D0021
(2) Shift to open side, pass the ANGLE1 then detect ANGLE2	0D0022
(3) Time out by PSW4 not changed to shift for close side	0D0023
(4) Shift to close side, pass the ANGLE1 then detect DETACH position	0D0024
4-2 Shift to ANGLE2 (fault PSW3)	
(1) Time out by PSW3 not change to shift for open side	0E0031
(2) Shift to open side, pass the ANGLE2 then detect ANGLE3	0E0032
(3) Time out by PSW3 not changed to shift for close side	0E0033
(4) Shift to close side, pass the ANGLE2 then detect ANGLE1	0E0034
4-3 Shift to ANGLE3 (fault PSW2)	
(1) Time out by PSW2 not changed to shift for open side	0F0041
(2) Shift to open side, pass the ANGLE3 then detect OPEN position	0F0042
(3) Time out by PSW2 not changed for shift for close side	0F0043
(4) Shift to close side, pass the ANGLE3 then detect ANGLE2	0F0044
5. PSW fault condition at initialize When all PSW is checked immediately after RESET, and the state of SWITCH which cannot be originally is detected, it is displayed as ERR 00.	000000

Flow until reading TOC of CD/CD-R/CD-RW

① FEED RETURN → Becomes DRVMUTE=H and the output of the IC604 driver becomes possible. Picking up is moved to surroundings on the inside until becoming REST SW=L. Afterward, moves in the direction of outer again and stops in the place in which became REST SW=H.

② OFFSET SELF ADJUSTMENT → FOCUS OFFSET, TRACKING OFFSET, and RF OFFSET are done, and OFFSET of RF AMP in IC603 is corrected.

③ LASER ON →

④ Pre SP KICK → 400ms turns the spindle motor before the focus search starts.

⑤ LENS UP → Lens UP of the pick is done. At this time, S character curve becomes about 2.0Vp-p by CTS-1000.

⑥ FOCUS ON → The down of the lens and FOCUS ONing are made.
Changes into CD-RW MODE, and serches for FOCUS in case of no FOCUS ON even if FOCUS search(UP DOWN) is done three times.

⑦ THE SPINDLE START → The spindle motor is rotated up to the number of necessary rotations.

⑧ TRAKING BALANCE → In the state of tracking OFF, do the self adjustment of wavy OFFSET of TE2 to 0. It takes time to adjust the one with a large gap of the traking balance of picking up. At this time, the racking error becomes about 2.8Vp-p by CTS-1000.

⑨ RF GAIN → In the state of traking OFF, do the self adjustment of the RF level of RF(TP601) to 1.0-1.2Vp-p. After adjusts,traking ON is done.

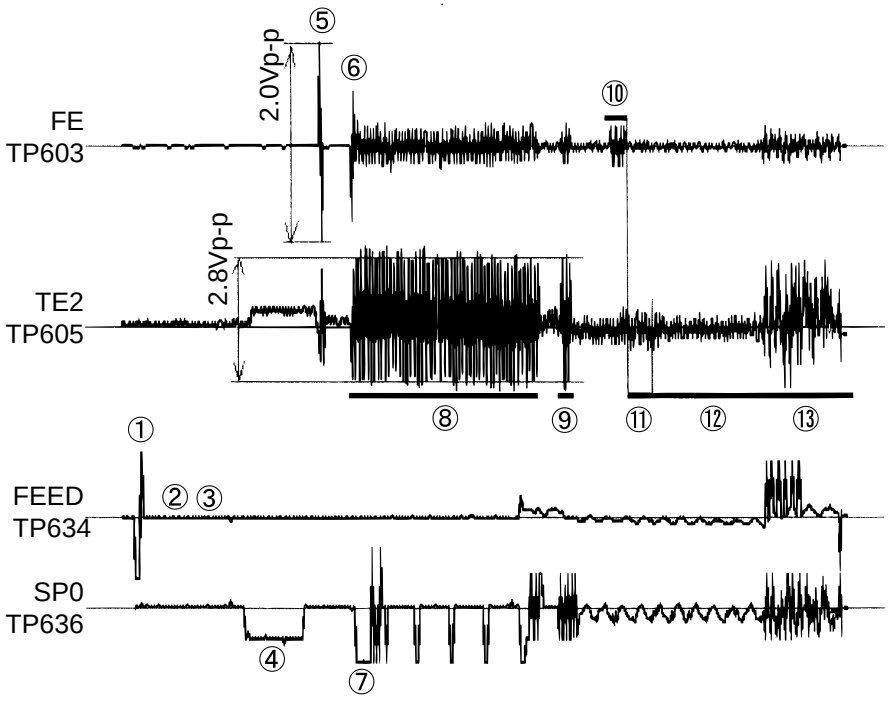
⑩ FOCUS GAIN → Do th eself adjustment of the gain intersection of the focus servo to 1.2kHz (300ms).

⑪ TRACKING → Do the self adjustment of the gain intersection of the focus servo to 1.2kHz. (300ms).

⑫ TOC READING → Time expands in DISC that the number of total tracks with CD-TEXT is a lot of.

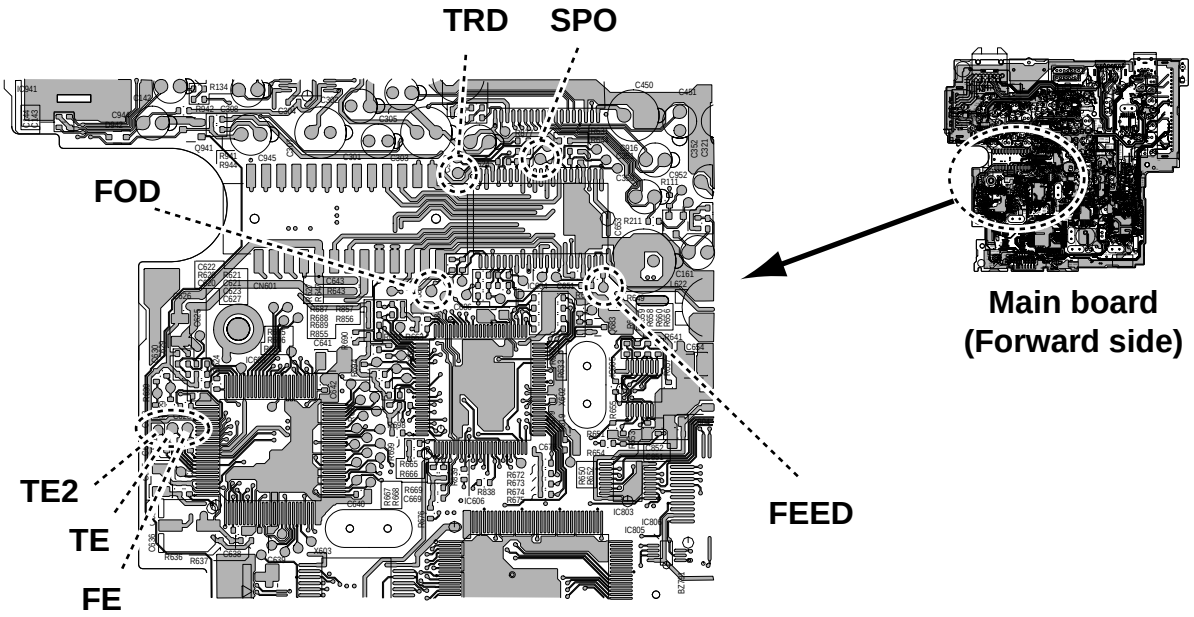
⑬ 1Tr. HEAD → It is a head of 1Tr., and the reproduction begins.

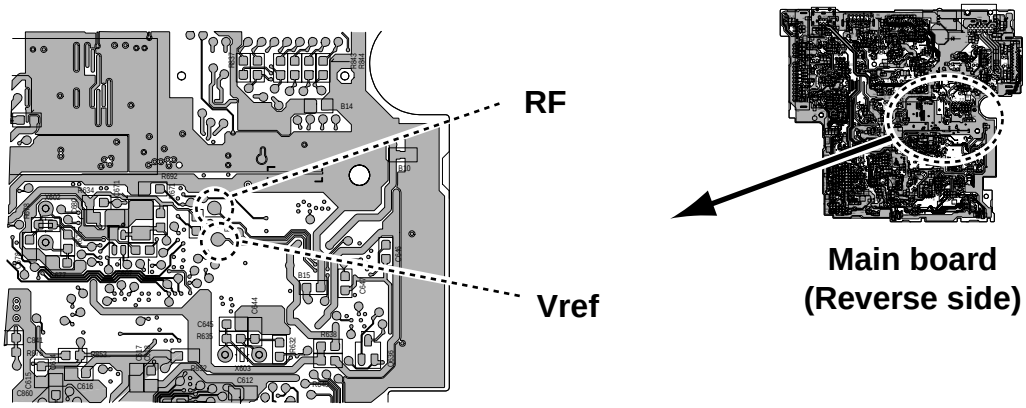
Shape of waves when based on Vref(TP602)



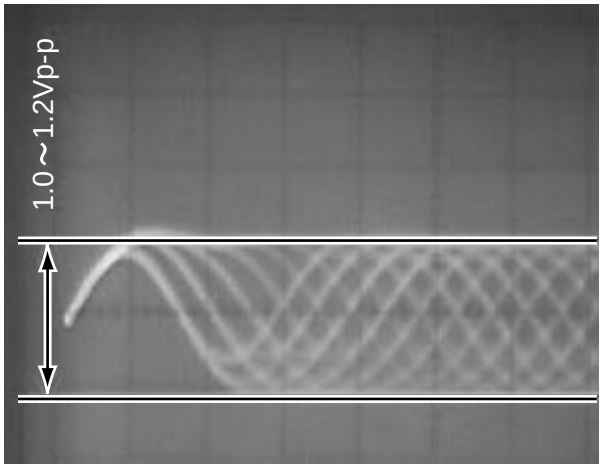
FE : Focus error signal
TE : T Tracking error signla
FEED : FEED deive signal
SPO : Spindle drive signal

■ Adjustment part





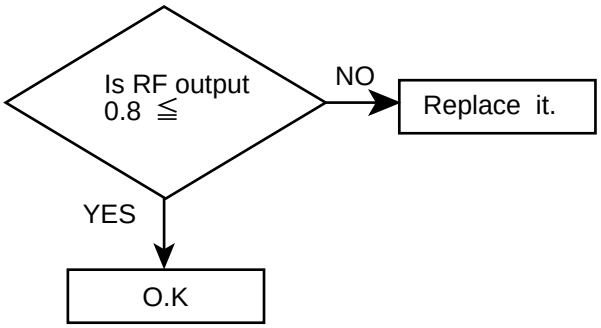
■ RF shape of waves



Maintenance of laser pickup

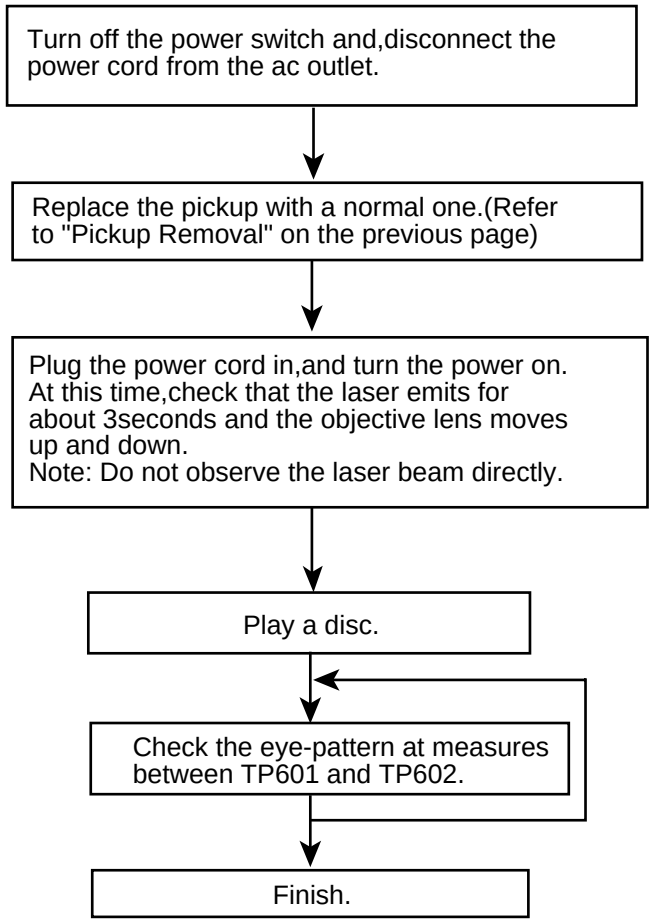
(1) Cleaning the pick up lens
Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.

(2) Life of the laser diode
When the life of the laser diode has expired, the following symptoms will appear.
(1) The level of RF output (EFM output:amplitude of eye pattern) will be low.



Replacement of laser pickup

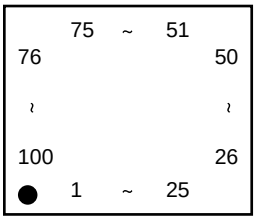
(3) Semi-fixed resistor on the APC PC board
The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power.Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.
If the laser power is lower than the specified value,the laser diode is almost worn out, and the laser pickup should be replaced.
If the semi-fixed resistor is adjusted while the pickup is functioning normally,the laser pickup may be damaged due to excessive current.



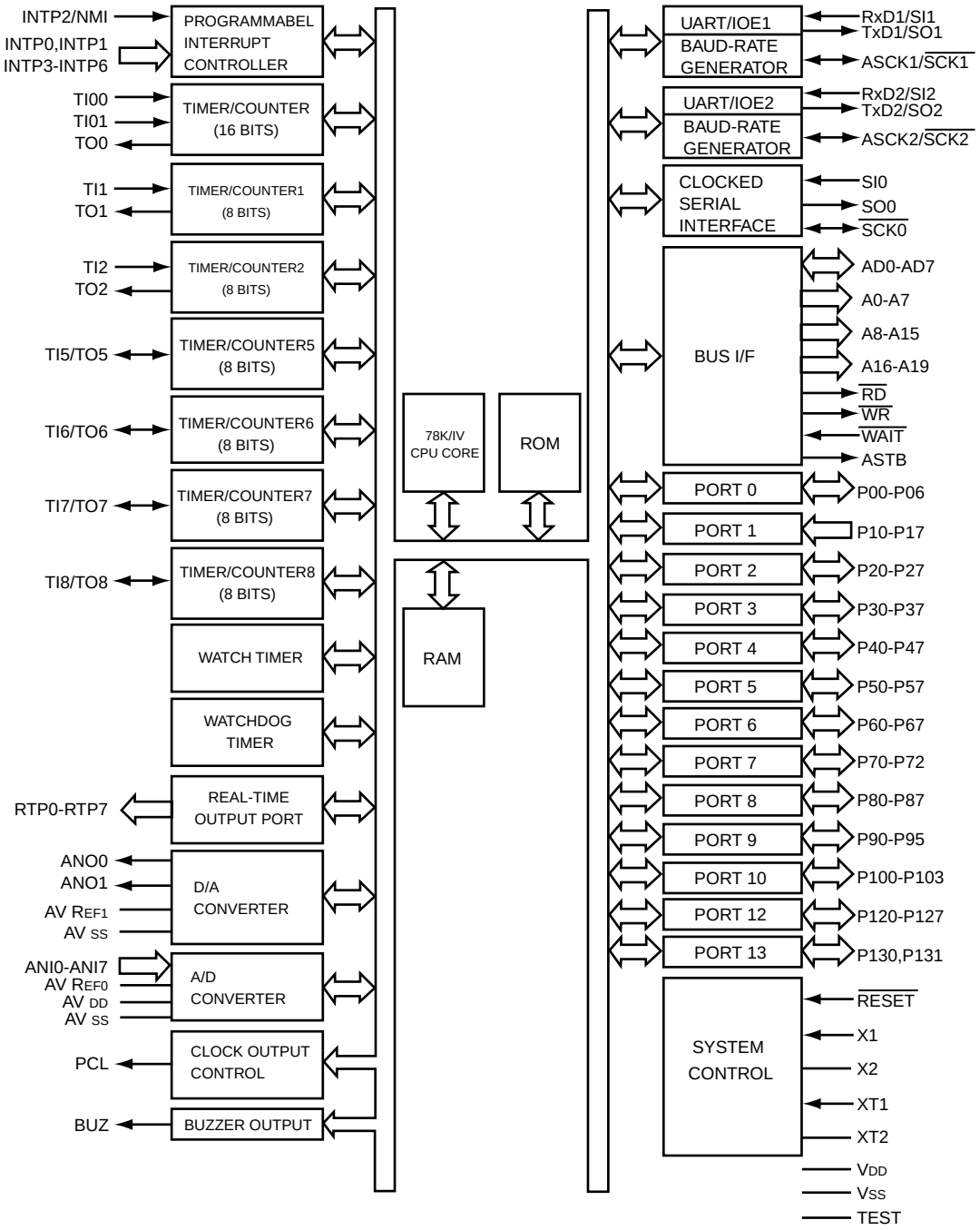
Description of major ICs

■UPD784215AGC145(IC701):MAIN CPU

1.Pin layout



2.Block diagram



UPD784215AGC145(1/2)

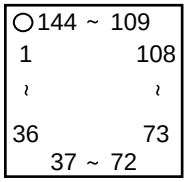
Pin No.	Symbol	I/O	Function
1	PREQ	O	Mechanism power supply ON/OFFdemand output("L":On demand)
2	AMUTE	O	Audio output MUTE control signal output ("L" :MUTE ON)
3		O	Non connected
4		O	Non connected
5		O	Non connected
6		O	Non connected
7	DIMMER-OUT	O	Unused output port
8	ANT PEM	O	Antenna remote output
9	VDD	-	5V connection
10	X2		Sub-clock 32.738MHz
11	X1	I	Sub-clock 32.738MHz
12	VSS	-	GND connection
13	XT2		Sub-clock 12.5MHz
14	XT1	I	Sub-clock 12.5MHz
15	RESET		Reset detection terminal
16		I	Non connected
17	BUS-INT	O	J-BUS signal interrupt input
18	PS2	I	POWER SAVE2 BACK UP synchronization. It is H input and stop mode.
19		I	Unused input port
20	RDS-SCK	I	RDS clock input
21	RDS-DA	I	RDS data input
22	REMOCON	I	Remote control signal input
23	AVDD	-	5V connction
24	AVREF0	-	5V connection
25	SD-ST	I	Station detector, stereo signal input. It is H and broadcasting station havingBroadcasting station,L:stereo
26	MRC DATA	I	MRC DATA input
27	KEY0	I	Key input 0
28	KEY1	I	Key input1
29	TEMP	I	Temperature data input for contrast correction
30	LEVEL	I	Level meter input
31	SQ	I	S.QUALITY level input
32	S.METER	I	S.METER level input
33	AVSS	-	GND connection
34	INLOCK	O	The LOCK detection output. At LOCK:H
35	NC	O	Unused output port
36	AVREF	-	5V connection
37	BUS-SI	I	J-BUS data input
38	BUS-SO	O	J-BUS data output
39	BUS-SCK	I/O	J-BUS clock I/O
40	(STAGE)	I	H:L:Initialization port
41	LCD-DA	O	Data output to LCD driver
42	LCD-CL	O	Clock output to LCD driver
43	LCD-CE	O	Chipenable output to LCD driver
44	BUZZER	O	Buzzer output
45	EPDAI	I	Communication data input of 12C
46	EPDAD	O	Communication data input of 12C
47	EPCLK	O	Communication data input of 12C
48	BUS-I/O	O	The J-BUS I/O switch output. When outputting :H,When inputting :L
49	PM0	O	Panel close side motor control signal output
50	PM1	O	Panel opening side motor control signal output

UPD784215AGC145(2/2)

Pin No.	Symbol	I/O	Function
51		O	Non connected
52		O	Non connected
53		O	Non connected
54	DETACH	I	The detach signal input. It is L of 200ms or more and operation mode. It is H and POWER SAVE.
55	VCR CONT	O	Signal output for VCR control
56	PNL SW1	I	Panel position detection switch one signal input.
57	PNL SW2	I	Panel position detection switch two signal input.
58	PNL SW3	I	Panel position detection switch three signal input.
59	PNL SW4	I	Panel position detection switch four signal input.
60	PNL SW5	I	Panel position detection switch five signal input.
61	PNL SW6	I	Panel position detection switch six signal input
62	AFCK	O	The Af check output. When you check AF:L.
63	SEEK/STOP	O	The auto seek stop switch output. At SEEK:H, STOP:L.
64	S MUTE	O	Software mute output for CF switch noise.
65	FM/AM	O	FM and the AM switch output. At FM:H,At AM:L
66	PLL-CE	O	CE output for IC control for PLL.
67	PLL-DO	O	Data output for IC control for PLL.
68	PLL-CLK	O	Clock output for IC control for PLL.
69	PLL-DI	I	Data input for IC control for PLL.
70	TEL-MUTE	I	Telephone ,ute detection input.
71	AMP KILL	O	POWER-AMP, ON/OFF switch output. H:OFF
72	VSS		GND connection
73	DIMMER-IN	I	Dimmer detection input. L:Dimmer ON
74	PS1	I	At POWER SAVE of POWER SAVE1.ACC and synchronization:L. When operating :H.
75	POWER	O	The POWER ON/OFF switch output. At the time of the POWER ON:H.
76	CD-ON	O	The CD power supply control signal output. At CD:H.
77	MUTE	O	The mute output. At the time of the MUTE ON:L.
78	W-LPF1	O	Sub woofer cutoff frequency control output 1
79	W-LPF2	O	Sub woofer cutoff frequency control output 2
80	W-MUTE	O	The mute output for the sub woofer. At the time of the MUTE ON:H.
81	VDD	O	5V connection.
82	VOL-DA	O	Data output for IC control for electronic volume.
83	VOL-CLK	O	Clock output for IC control electronic volume.
84	CF-SEL	O	Signal output for FM belt region filter switch.
85	PMKICK	O	Signal output for panel motor kick
86	EMPH	O	The CD emphasis output. When turning.At On:H.
87		O	Non connected
88	VOL-1	I	Pulse which rotation volume pulse signal inputs, and becomes judgment of change actually.
89	VOL-2	I	rotation volume pulse signal input
90	(J/R)	I	H:J version and L:R version
91	BUCK	O	Non connected
92	CCE	O	Non connected
93	LSI RST	O	CDLSI reset signal output
94	TEST		GND connection
95		O	Non connected
96		O	Non connected
97		O	Non connected
98		O	Non connected
99	(DISC SEL)	O	Non connected
100	SW1	I	Panel SW1

■UPD63711AGC(IC603):RF Servo amp

1.Pin layout



2.Pin function

UPD63711AGC(1/3)

Pin No.	Symbol	I/O	Function
1	VSSO	-	It is GND of the logic circuit.
2	ZRASO	O	It is RFOK signal output terminal.
3	ZCASO	I	Reset signal input terminal. (Active row)
4	ZCAS1	I	Command/parameter identification signal input terminal A0=L:STB active=Address register set. A0=H:STB active= Parameter set.
5	VSSO	I	The data strove signal input terminal. It is signal to de the latch in LSI as for the cereal data.
6	ZOE	I	The clock signal input terminal to input and output the cereal data. Input data from terminal SI is taken by standing up about this signal, and the cereal data from the terminal SO is output with go down.
7	ZUWE	O	The cereal data and the status signal are output.
8	ZLWE	I	Cereal data input terminal.
9	VSSO	I	The crystal oscillation control terminal. Please input the reset signal before stopping the crystal oscillation. Moreover, the crystal oscillation is steady and input the reset signal, please when moves from the state of the crystal oscillation stop to the ordinary mode. XTALEN=L:ordinary mode XTALEN=H:Crystal oscillation stop.
10	RA0	-	Positive power supply supply terminal to logic circuit.
11	RA1	-	Positive power supply supply terminal to D/A converter.
12	RA2	O	R-ch audio signal output terminal.
13	RA3	-	It is D/A converter GND.
14	RA4	-	The outside credit capacitor connection terminal for SCF regulator.
15	RA5	-	It is D/A converter GND.
16	RA6	O	L-ch audio signal output terminal.
17	RA7	-	Positive power supply supply terminal to D/A converter.
18	VDD0	O	Output terminal of right channel voice data. PWM output.
19	VSS0		
20	RA8	O	Left channel voice data audio output terminal. PWM output.
21	IO0		
22	IO1	-	Positive power supply supply terminal to crystal oscillation circuit.
23	IO2	O	Crystal departure pendulum connection terminal (Output)
24	IO3	I	Crystal departure pendulum connection terminal (Input)
25	IO4	-	It is GND of the crystal oscillation circuit.
26	IO5	-	Positive power supply supply terminal to logic circuit.
27	VSSO	O	The output terminal of priemphasis information in sub code Q. When the emphasis is added, high level is output. Polarity can be switched by the command. F6H LSB EP=0:Normal output EP=1:Reversing output.
28	IO6	O	Flag output terminal which shows that data under output is composed by data which cannot be corrected.(active high)
29	IO7	I	The cereal data input terminal to building DAC into. When DSP etc. are not connected with latter part, it should be short with the terminal DOUT.
30	IO8	O	It is an output terminal of the cereal voice data.
31	IO9	I	Cereal clock input terminal to building DAC into. The output voice data changes from DOUT by standing up about this clock. The system connected with latter part must take data by standing up about this signal.
32	IO10	O	The output voice data changes from DOUT by standing up about this clock.The system connected with latter part must take data by standing up about this signal.

UPD63711AGC(2/3)

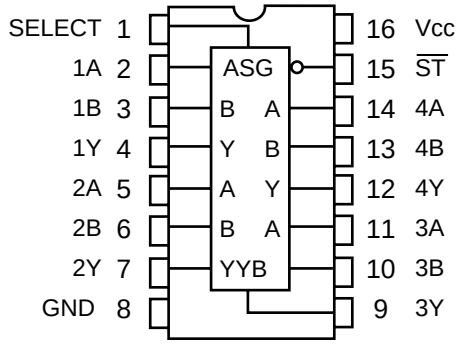
Pin No.	Symbol	I/O	Function
33	IO11	I	LRCK signal input terminal to building DAC into.
34	IO12	O	Signal which distinguishes left channel/right channel of voice data output from DOUT.
35	IO13	O	Terminal (88.2kHz)(WDCK)of the output of the frequency signal twice defect detection output terminal(HOLD) LRCK HOLD/WDCK can be switched with the microcomputer.
36	VSSO	O	Terminal of output of data of Digital audio interface.
37	VDD1	-	It is GND of the logic circuit.
38	IO14	O	Buffer ring output terminal of oscillation.
39	IO15	I	The state of this terminal is output to Bit5 of the status output.
40	DREQ	-	Positive power supply supply terminal to logic circuit.
41	DRESP	O	It is EFM-synchronous detection signal.becomes high-level when the
42	IOP7	O	output of the synchronous pattern detection signal and the frame counter is corresponding by the EFM recovery part, and becomes a row level at the disagreement.
43	IOP6	O	Mirror output terminal. (MIRR).It is a frame synchronous signal of PLL system. The one that a basic frequency (44.1kHz)of the reading signal obtained in PLL system was divided makes almost equally to the synchronization(7.35kHz) of one frame. (WFCK)MIRR/WFCK can be switched with the microcomputer.
44	IOP5	O	the terminal for the monitor of the bit clock. When PLL is locked, the go down edge of the EFM signal and this signal locks.
45	IOP4	-	it is GND of the logic circuit.
46	IOP3	O	The output terminal which shows the C1 error correction result. Even go down of RFCK is fixed.
47	IOP2		
48	IOP1	O	It is an output terminal which shows the C2 error correction result. Even of RFCK is fixed.
49	IOP0		
50	HDBDIR		
51	DVDD	-	Positive power supply supply terminal to logic circuit.
52	PACK	O	It is PACK synchronous signal shows the head of packing.
53	TSO	O	It is a cereal output terminal of the CD-TEXT data.
54	TSI	I	It is a serial input terminal of the CD-TEXT control parameter.
55	TSCK_B	I	Cereal clock input terminal of CD-TEXT.
56	TSTB_B	I	Terminal of input of parameter strove signal of CD-TEXT.
57	DGND	-	It is GND of the logic circuit.
58	TEST0	I	It is a test terminal. Please connect with GND usually.
59	TEST1		
60	ATEST	O	It is a test terminal. Please make to the opening usually.
61	AGND	-	It is GND of an analog circuit.
62	FD	O	Focus drive output terminal.
63	TD	O	Tracking drive output terminal.
64	SD	O	Thread drive output terminal.
65	MD	O	Spindle drive output terminal.
66	DACO	O	It is DAC output terminal for the adjustment. A set value of CRAM7FH is output.
67	FBAL	O	It is DAC output terminal for the adjustment. A set value of CRAM7CH is output (built-in RF FE amplifier offeset).
68	TBAL	O	It is DAC output terminal for the adjustment. A set value of CRAM7DH is output.
69	TEVCA	O	It is DAC output terminal for the adjustment. A set value of CRAM7EH is output (built-in RF TE amplifier offset).
70	AVDD	-	It is a positive power supply supply terminal to an analog circuit.
71	EFM	O	EFM signal output terminal.
72	ASY	I	It is a standard voltage input terminal of the EFM comparator.
73	C3T	-	Capacitor connection terminal for 3T detection.
74	RFI	I	RF signal input terminal for EFM data generation.
75	AGCO	O	RF signal output terminal after gain is adjusted.
76	AGCI	I	Input terminal of RF-AGC amplifier.
77	RFO	O	Output terminal of RF saming amplifier.

UPD63711AGC(2/2)

Pin No.	Symbol	I/O	Function
78	EQ2	-	Equalizer part connection terminal of RF amplifier.
79	EQ1		
80	RF	I	Reversing input terminal of RF saming amplifier.
81	AGND	-	It is GND of an analog circuit.
82	A	I	Photo detector A input terminal.
83	C	I	Photo detector B input terminal.
84	B	I	Photo detector C input terminal.
85	D	I	Photo detector D input terminal.
86	F	I	Photo detector F input terminal.
87	E	I	Photo detector E input terminal.
88	AVDD	-	Positive power supply supply terminal to analog circuit.
89	REFOUT	O	reference potential output terminal.
90	FE	I	Focus make an error amplifier reversing input terminal.
91	FEO	O	Focus Allah amplifier output terminal.
92	TE	I	Tracking make an error amplifier reversing input terminal.
93	TEO	O	Tracking error amplifier output terminal.
94	TE2	O	Terminal to which tracking error after amplifies is output.
95	TEC	I	The tracking comparator input terminal. The tracking error signal which cuts the DC element is input. The tracking 0 crossing is detected by using this signal in LSI.
96	AGND	-	it is GND of an analog circuit.
97	PD	I	It is a terminal of the input of the detection signal of PD for the LD output monitor.
98	LD	O	LD control current output terminal.
99	PN	I	It is a control polarity set value of the APC circuit.
100	AVDD	-	Positive power supply supply terminal to analog circuit.

■ TC74VHC157FT-X(IC803):DAC SW

1.Pin lauout



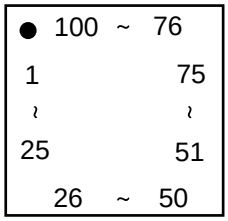
2.Pin function

INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X:Don't Care

■UPD703031AGC012(IC606):SUB CPU

1.Pin layout



2.Pin function

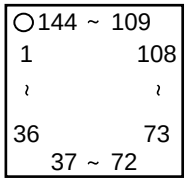
Pin No.	Symbol	I/O	Function
1	TSI	O	CD TEXT control parameter cereal output
2	TSCK	O	CD TEXT control cereal clock output
3	JBSO	O	JBUS cereal data output
4	JBSI	I	JBUS cereal data input
5	JBCK	I/O	JBUS cereal clock I/O
6	EVDD	-	5V(Power supply for port for I/O)
7	EVSS	-	GND(GND for port for I/O)
8	TSTB	O	CD-TXET parameter strobe signal output
9	XRESET	O	LSI reset output
10	MIRR	I	MIRR signal input(H:Specular)
11	AO	O	Command:L/parameter:H switch signal output
12	SO	I	DSP cereal data input
13	SI	O	DSP cereal data input
14	SCK	O	DSP cereal data clock output
15	WSEN	O	Internal CD/DC operation of MP3 operation & beginning
16	DSPRST	O	DSP RESET:L
17	SWAIT	I	WAIT signal input from DECODER
18	VPP	-	FLASH writing power supply
19	SA4	O	DECODER address bus output
20	SA5	O	DECODER address bus output
21	SA6	O	DECODER address bus output
22			(Non connected)
23	STB	O	DSP cereal data latch output
24	DRVMUTE	O	Servo driver MUTE control signal output ("L":MUTE ON)
25	LOAD1	O	Loading drive
26	LOAD2	O	Loading drive
27	SAO	O	DECODER address bus output
28	SA1	O	DECODER address bus output
29	SA2	O	DECODER address bus output
30	SA3	O	DECODER address bus output
31	RESET	I	Microcomputer reset terminal("L":Reset)
32	XT1	I	Sub-clock
33	XT2	-	Sub-clock
34		-	
35		-	The main clock crystal oscillation machine
36		I	The main clock crystal oscillation machine(20MHz)
37	VSS	-	5V
38	VDD	-	GND
39	CLKOUT	O	Internal system clock output(Non connect)
40	WR	O	DECODER data writing
41	---	O	(Non connected)
42	---	O	(Non connected)
43	RD	O	DECODER data reading
44	---	O	Address bus enable(Non connected)
45	JBCONT	O	JBUS I/O switch
46	PON	I	Mechanism power supply ON:L
47	AD0	I/O	DECODER I/O data bus
48	AD1	I/O	DECODER I/O data bus
49	AD2	I/O	DECODER I/O data bus
50	AD3	I/O	DECODER I/O data bus

UPD703031AGC012(2/2)

Pin No.	Symbol	I/O	Function
51	AD4	I/O	DECODER I/O data bus
52	AD5	I/O	DECODER I/O data bus
53	AD6	I/O	DECODER I/O data bus
54	AD7	I/O	DECODER I/O data bus
55	BVDD	-	5V
56	BVSS	-	GND
57	---	O	Non connected
58	---	O	Non connected
59	---	O	Non connected
60	---	O	Non connected
61	---	O	Non connected
62	---	O	Non connected
63	---	O	Non connected
64	---	O	Non connected
65	MD	O	DAC mode control data
66	MC	O	DAC mode control clock
67	ML	O	DAC mode control latch
68	MP3SEL	O	MP3/CD-DA switch SW L:CD H:MP3
69	PREQ	O	Mechanism power supply ON/OFF demand output ("L":On demand)
70	AMUTE	O	Audio output MUTE control signal output ("L":MUTE ON)
71	AVDD	-	5V(Power supply for AD converter)
72	AVSS	-	GND(GND for AD converter)
73	AVREF	-	5V(Standard voltage for AD converter)
74	PDET	I	BACK UP power supply detection)
75	SW2	I	SW2 mechanism switch
76	SW3	I	SW3 mechanism switch
77	SW4	I	SW4 mechanism switch
78	REST	I	Surroundings position detection switch(L:Surroundings)
79	RFOK	I	RFOK signal input
80	REQ	I/O	Data demend
81	EXT	I	H:Export L:For country 8cm CD
82	ADIN0	I	Test key input 0(A/D input)
83	ADIN1	I	Test key input 1(A/D input of one)
84	ADIN2	I	Test key input 2(A/D input of two)
85	ADIN3	I	Test key input 3(A/D input of three)
86	---	O	(Non connected)
87	CONT+B	I	LS15V On power supply control signal and JBUS control signal input
88	SW1	I	SW1 mechanism switch
89	PACK	I	PACK synchronous signal of CD-TEXT
90	INT0	I	DECODER interrupt request
91	INT1	I	DECODER interrupt request
92	JBINT	I	J-BUS interrupt signal input
93	TESTMODE	I	L:Test mode shift
94	12CD	I/O	12C data line
95	---	O	(Non connected)
96	12CC	I/O	12C clock line
97	RXD0	I	FLASH writing cereal data input
98	SID	O	MP3 cereal data output/FLASH writing cereal data output
99	SIC	O	MP3 cereal clock output/FLASH writing cereal clock output
100	TS0	I	CD-TEXT data serial input

■LC895199K-ND2(IC601):CD-ROM decoder

1.Pin layout



2.Pin function

LC895199K-ND2(1/3)

Pin No.	Symbol	Function
1	VSSO	
2	ZRASO	RAS signal output terminal to buffer DRAM
3	ZCASO	CAS signal output 0 terminal to buffer DRAM(0 is used usually)
4	ZCAS1	CAS signal output terminal 1 to buffer DRAM
5	VSSO	
6	ZOE	Buffer DRAM output enable
7	ZUWE	Buffer DRAM upper write enable
8	ZLWE	Buffer DRAM lower write enable
9	VSSO	
10	RA0	Address signal output terminal to data buffer DRAM
11	RA1	
12	RA2	
13	RA3	
14	RA4	
15	RA5	
16	RA6	
17	RA7	
18	VDD0	5.0V
19	VSS0	
20	RA8	Address signal output terminal to data buffer DRAM
21	IO0	Data I/O terminal to data buffer DRAM. With built-in pull-up resistor
22	IO1	
23	IO2	
24	IO3	
25	IO4	
26	IO5	
27	VSSO	
28	IO6	Data I/O terminal to data buffer DRAM. With built-in pull-up resistor
29	IO7	
30	IO8	
31	IO9	
32	IO10	
33	IO11	
34	IO12	
35	IO13	
36	VSSO	
37	VDD1	3.3V
38	IO14	Data I/O terminal to data buffer DRAM.With buolt-in pull-up resistor
39	IO15	
40	DREQ	
41	DRESP	
42	IOP7	General-purpose I/O port
43	IOP6	
44	IOP5	
45	IOP4	
46	IOP3	
47	IOP2	
48	IOP1	
49	IOP0	
50	HDBDIR	

LC895199K-ND2(2/3)

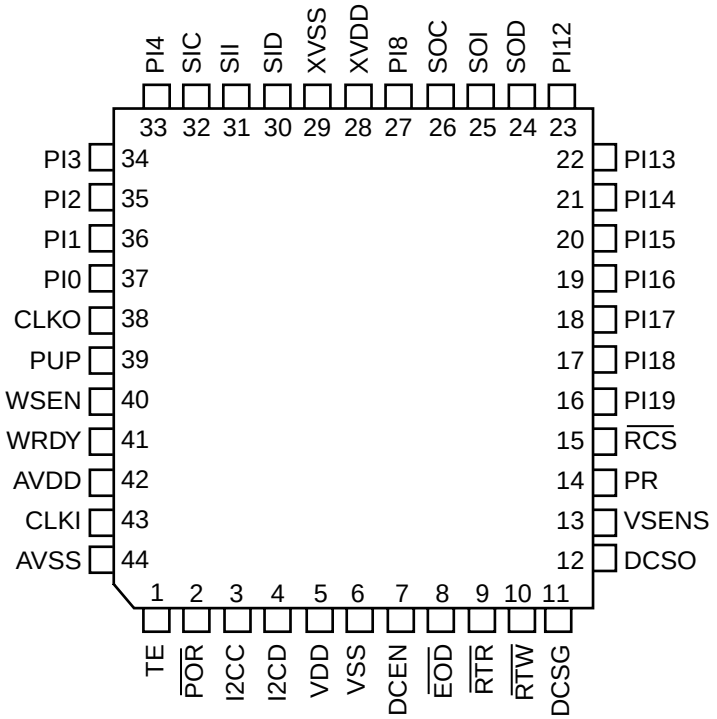
Pin No.	Symbol	Function
51	TEST0	The terminal TEST.Please connect with VSS
52	XTALCK	X'tal oscillation circuit input terminal
53	XTAL	X'tal oscillation circuit output terminal
54	VDD0	5.0V
55	VSS0	
56	MCK	1/1,2/2,STOP output terminal of XTALCK
57	TEST1	The terminal TEST. Please connet with VSS
58	DSDATA	DAC output terminal
59	DLRCK	
60	DBCK	
61	C2PO	Terminal for CD-DSP I/F
62	SDATA	
63	BCK	
64	LRCK	
65	EXCK	SUB-CODE I/O terminal
66	WFCK	
67	SBSO	
68	SCOR	
69	PLL1	Relation connection of PLL terminal
70	PLL2	
71	PLL3	
72	VSS0	(It is analog VSS in version LC895199 with built-in PLL)
73	VDD1	3.3V (It is analog VDD in version LC895199 with buikt-in PLL)
74	ZRESET	LSI reset terminal
75	MCK3	1/1, 1 /5, 2/5, 1/512, and STOP output terminal of XTALCK
76	CSCTRL	Active Lo and Hi selection terminal on MC(microcontroller) side CS
77	ZRO	Reading data of MC(microcontroller) signal input terminal
78	ZWR	Writing data of MC(microcontroller) signal input terminal
79	ZCS	Register chip selection signal input terminal from MC(microcontroller)
80	SUA0	MC(microcontroller) register selection signal terminal
81	SUA1	
82	SUA2	
83	SUA3	
84	SUA4	
85	SUA5	
86	SUA6	
87	D0	MC(microcontroller) data signal terminal.With buit-in puul-up resistor.
88	D1	
89	D2	
90	VDD0	5.0V
91	VSS0	
92	D3	MC(microcontroller) data signal terminal. With buit-in pull-up resistor.
93	D4	
94	D5	
95	D6	
96	D7	
97	ZINTO	Interrupt request signal output terminal to MC(microcontroller)
98	ZINT1	
99	ZSMAIT	WAIT signal to MC(microcontroller)
100	ZRSTCPU	Reset signal to CPU
101	CSEL	ATAPI control signal
102	ZHRST	ATAPi data bus
103	ATPINSEL	Terminal ATAPI arrangement select terminal. Connects with VDD0
104	ZDASP	ATAPI data bus
105	ZCS3FX	
106	ZCS1FX	
107	DA2	
108	VSS1	
109	VDD1	3.3V

LC895199K-ND2(3/3)

Pin No.	Symbol	Function
110	DAO	ATAPI data bus
111	ZPDIAG	
112	DA1	
113	ZIOCS16	
114	HITRQ	
115	ZDMACK	
116	VSS1	
117	IORDY	ATAPI data bus
118	ZDIOR	
119	ZDIOR	
120	DMARQ	
121	VSS1	
122	DD15	ATAPi data bus
123	DDO	ATAPi control signal
124	DD14	ATAPI control signal
125	DD1	
126	VDDO	5.0V
127	VSS1	
128	DD13	ATAPI control signal
129	DD2	
130	DD12	
131	DD3	
132	VSS1	
133	DD11	ATAPI control signal
134	DD4	
135	DD10	
136	VSS1	
137	VDD0	5.0V
138	DD5	ATAPI control signal
139	DD9	
140	DD6	
141	VSS1	
142	DD8	
143	DD7	
144	VDD1	3.3V

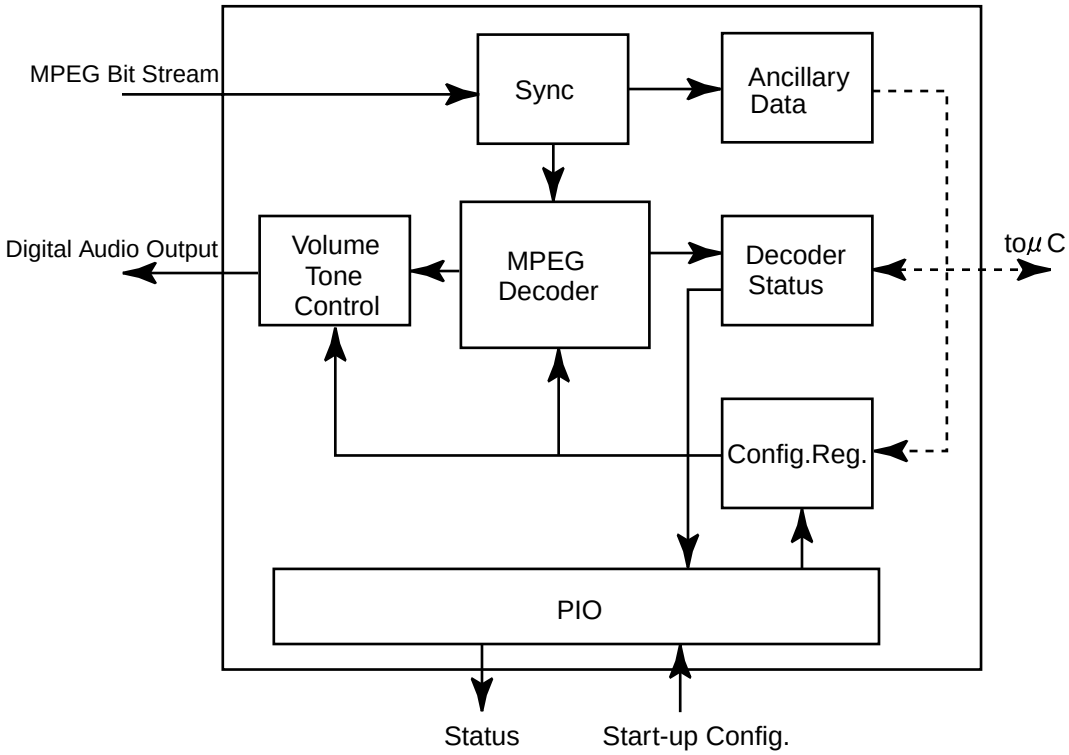
■MAS3507D-QG-G10 (IC806) :MP3 decoder

1.Pin layout



(TOP VIEW)

2.Block diagram



3.Pin function

MAS3507D-QG-G10(1/2)

Pin no.	Symbol	I/O	Function
1	TE	I	Test Enable
2	POR	I	Reset, Active Low
3	I2CC	I/O	I^2C Clock Line
4	I2CD	I/O	I^2C Data Line
5	VDD	Supply	Positive Supply for Digital Parts
6	VSS	Supply	Ground Supply for Digital Parts
7	DCEN	I	Enable DC/DC Converter or Voltage Supervision
8	EOD	OUT	PIO End of DMA, Active Low
9	RTR	OUT	PIO Ready to Read, Active Low
10	RTW	OUT	PIO Ready to Write, Active Low
11	DCSG	Supply	DC Converter Transistor Ground
12	DCSO	O	DC Converter Transistor Open Drain
13	VSENS	I	DC Converter Voltage Sense
14	PR	IN	PIO DMA Request Read/$\overline{\text{Write}}$
15	PCS	IN	PIO Chip Select, Active Low
16	PI19	IN/OUT	PIO Data(19) i)Demand Pin in SDI mode ii)data bit(7),MSB in PIO DMA input mode
17	PI18	IN/OUT	PIO Data(18) i)MPEG header bit11-MPEG ID(SDI mode) ii)data bit(6) in PIO DMA input mode
18	PI17	IN/OUT	PIO Data (17) i)MPEG header bit 12-MPEG ID(SDI mode) ii)data bit(5) in PIO DMA input mode
19	PI16	IN/OUT	PIO Data(16) i)SIC,alternative input for SIC(SDI mode) ii)data bit(4) in PIO DMA input mode
20	PI15	IN/OUT	PIO Data(15) i)SII, alternative input for SII(SDI mode) ii)data bit(3) in PIO DMA input mode
21	PI14	IN/OUT	PIO Data(14) i)SID, alternative input for SID (SDI mode) ii)data bit(2) in PIO DMA input mode
22	PI13	IN/OUT	PIO data(13) i)MPEG header bit 13-Layer ID (SDI mode) ii)data bit(1) in PIO DMA input mode
23	PI12	IN/OUT	PIO Data (12) i)MPEG header bit 14-Layer ID (SDI mode) ii)data bit(0) in PIO DMA input mode
24	SOD	O	Serial Output Data
25	SOI	O	Serial Output Frame Identification
26	SOC	O	Serial Output Clock
27	PI18	IN/OUT	Start-up [1)] : Clock output scaler on/off Operation : MPEG CRC error
28	XVDD	Supply	Positive Supply of Output Buffers
29	XVSS	Supply	Ground of Output Buffers
30	SID	I	Serial Input Data
31	SII	I	Serial Input Frame Identification
32	SIC	I	Serial Input Clock
33	PI4	IN/OUT	Start-up [1)] : Select SDI/PIODMA input mode Operation : MPEG-Frame Sync
34	PI3	IN/OUT	Start-up [1)] : Enable Layer 3 / Disable Layer 3 decoding Operation : MPE Gheader bit 20(Sampling Frequency)
35	PI2	IN/OUT	Start-up [1)] : Enable Layer 2 / Disable Layer 2 decoding Operation : MPEG header bit 21(Sampling Frequency)

3.Pin function

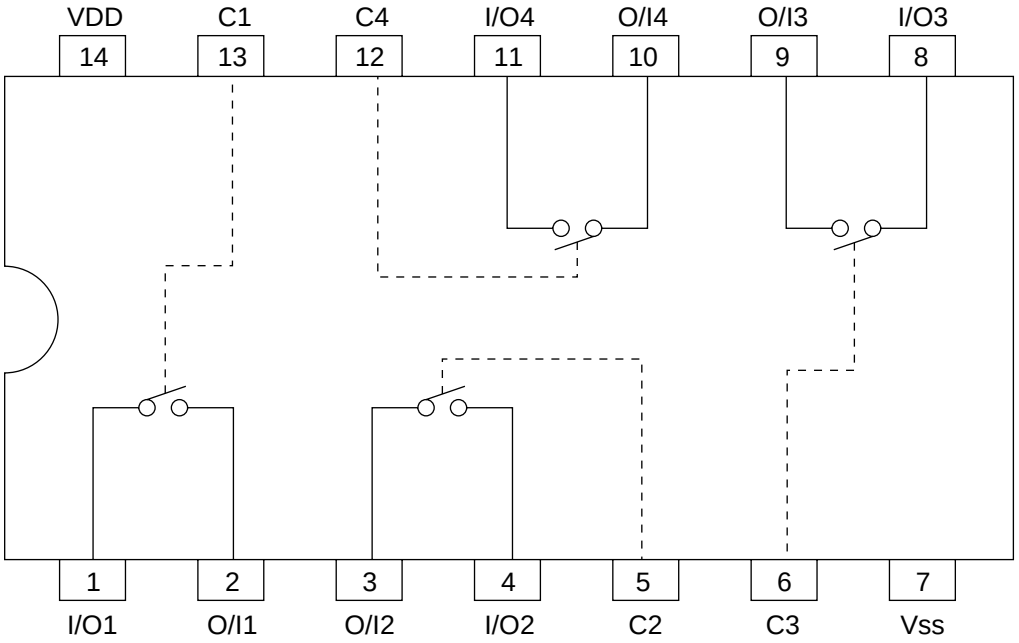
MAS3507D-QG-G10(2/2)

Pin no.	Symbol	I/O	Function
36	PI1	IN/OUT	Start-up [1]: SDO Select 32 bit mode / 16 bit I ² S mode Operation : MPEG header bit 30(Emphasis)
37	P0	IN/OUT	Start-up [1]: Select Multimedia mode / Broadcast mode Operation MPEG header bit 31 (Emphasis)
38	CLKO	O	Clock Output (normal 24.576 MHz)
39	PUP	O	Power Up, i.e.Status of Voltage Supervision
40	WSEN	I	WS Enable : Enable DSP
41	ERDY	O	WSEN=0 : Valid clock input at CLKI WSEN=1 : Clock synthesizer PLL locked
42	AVDD	Supply	Supply for Analog Circuits
43	CLKI	I	Clock Input
44	AVSS	Supply	Ground Supply for Analog Circuits

[1] Start-up configuration see Table 2.7.3. in (1)

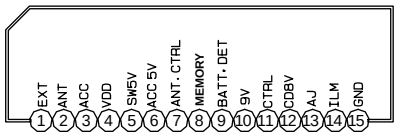
■BU4066BCFV-X (IC322) : Quad analog switch

1. Pin layout & Block diagram

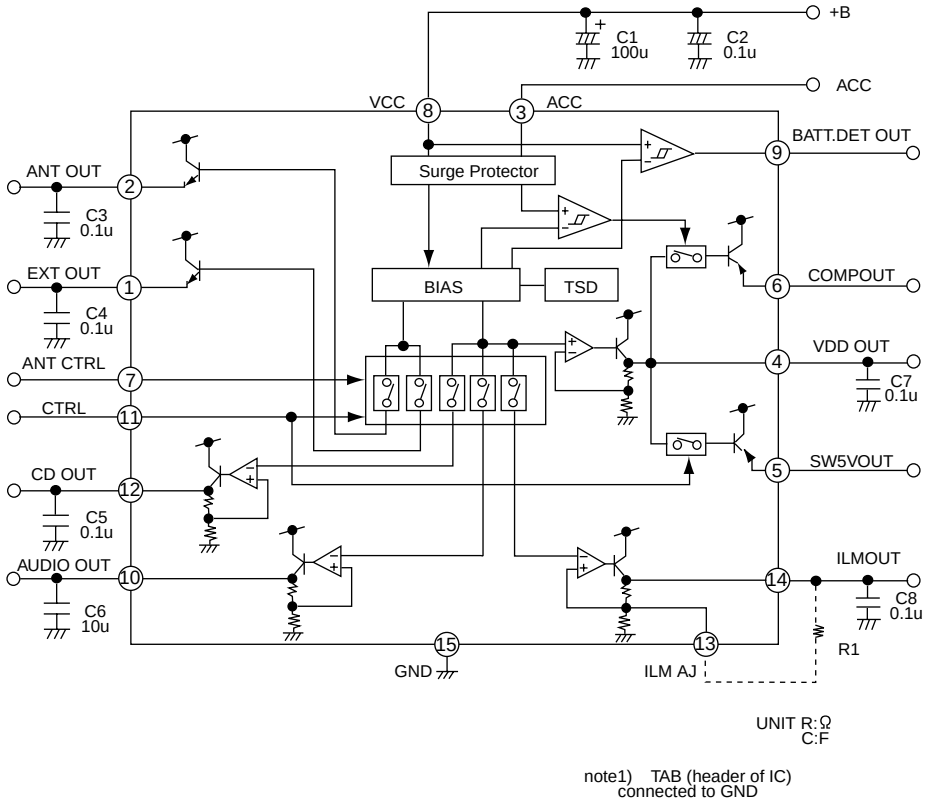


■ HA13164 (IC961) : Regulator

1.Terminal layout



2.Block diagram

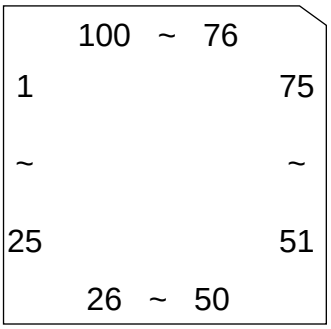


3.Pin function

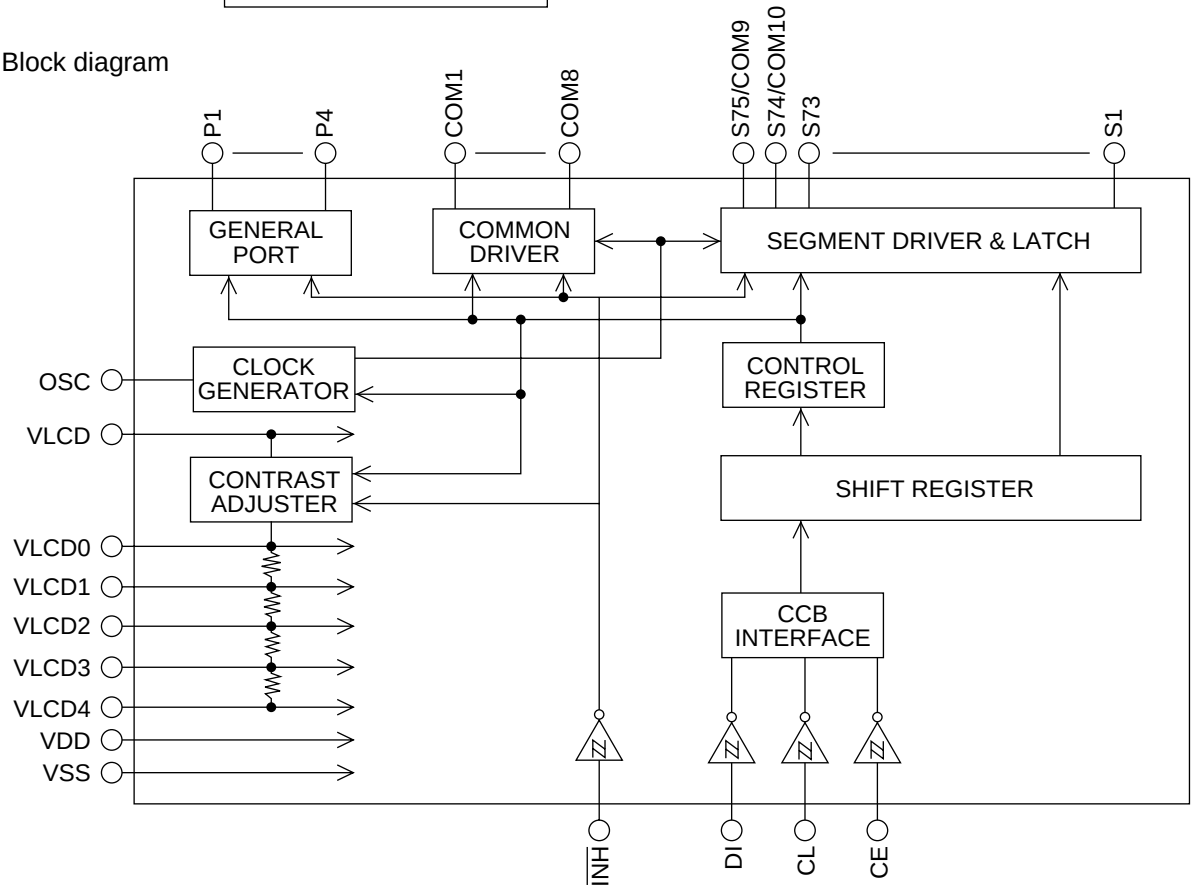
Pin No.	Symbol	Function
1	EXT	Output voltage is VCC-1 V when M or H level applied to CTRL pin.
2	ANT	Output voltage is VCC-1 V when M or H level to CTRL pin and H level to ANT-CTRL.
3	ACC	Connected to ACC.
4	VDD	Regular 5.7V.
5	SW5V	Output voltage is 5V when M or H level applies to CTRL pin.
6	ACC5V	Output for ACC detector.
7	ANT CTRL	L:ANT output OFF , H:ANT output ON
8	MEMORY	Connected to VCC.
9	BATT DET	Low battery detect.
10	9V	Output voltage is 9V when M or H level applied to CTRL pin.
11	CTRL	L:BIAS OFF, M:BIAS ON, H:CD ON
12	CD8V	Output voltage is 8V when H level applied to CTRL pin.
13	AJ	Adjustment pin for ILM output voltage.
14	ILMI	Output voltage is 10V when M or H level applies to CTRL pin.
15	GND	Connected to GND.

■ LC75878W (IC501) : LCD driver

1. Pin layout



2. Block diagram

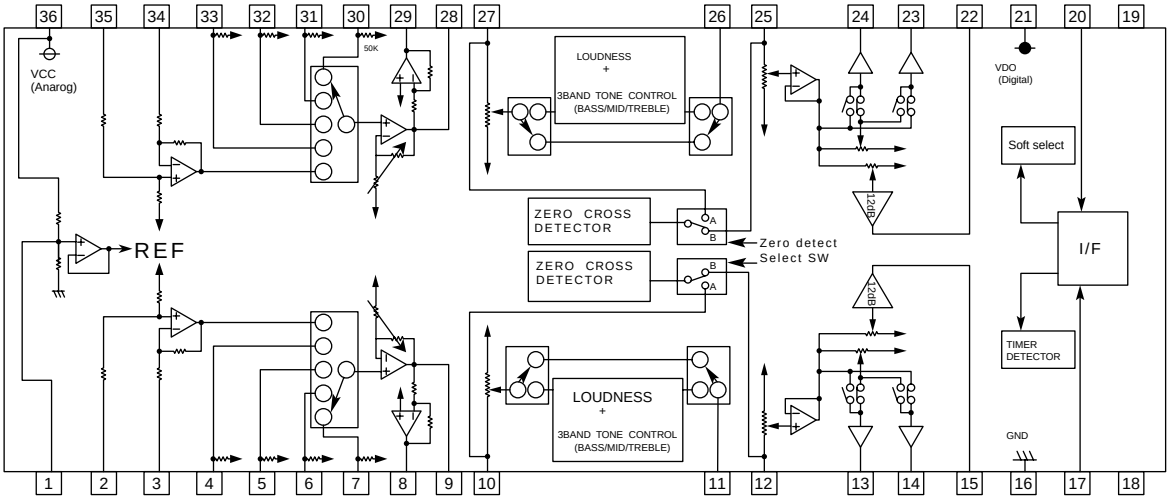


3. Pin function

No.	Symbol	I/O	Function
1~73	SEG1~SEG73	O	Segment driver output pin.
74	SEG74	O	Segment driver output pin.
75	SEG75	O	Segment driver output pin.
76~83	COM8~COM1	O	Common driver output pin.
84~87	P1~P4	O	General-purpose output pin.
88	VDD	-	Logic block power supply pin.
89	VLCD	-	LCD driver power supply pin.
90	VLCD0	O	LCD driver bias 4/4 voltage (H-level) power pin.
91	VLCD1	I	LCD driver bias 3/4 voltage (intermediate level) power pin.
92	VLCD2	I	LCD driver bias 2/4 voltage (intermediate level) power pin.
93	VLCD3	I	LCD driver bias 1/4 voltage (intermediate level) power pin.
94	VLCD4	I	LCD driver bias 0/4 voltage (L-level) power pin.
95	VSS	-	Power supply pin to connect to ground.
96	OSC	I/O	Oscillator pin.
97	LCD RESET	I	Display off, general-purpose output port「L」fixed input pin.
98	CE	I	Chip enable
99	CL	I	Synchronization clock
100	DI	I	Transfer data

■ M61508FP-X (IC911) : E. volume

1. Pin layout & Block diagram

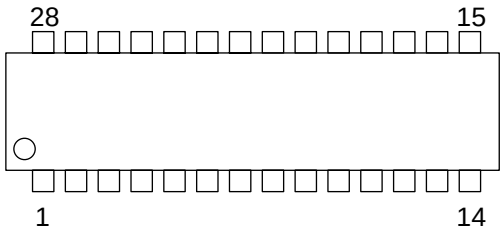


2. Pin function

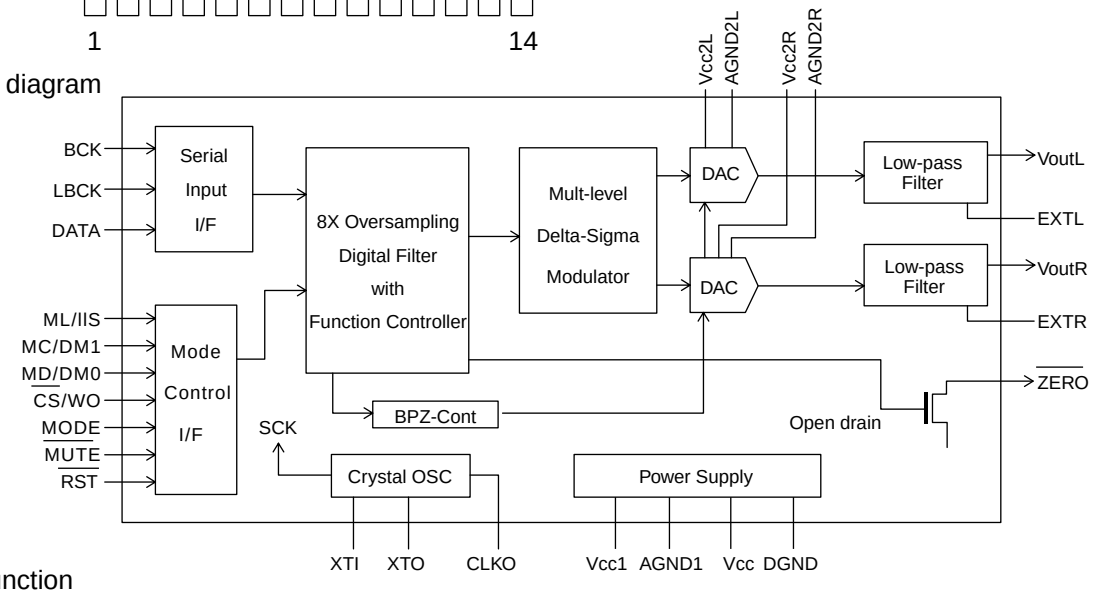
Pin No.	Symbol	Function
1	REF	Grand for IC signal
2	DEFP IN1	Differential motion amp. Positive terminal
3	DEFN IN1	Differential motion amp. Negative terminal
4	INA1	Input terminal of input selector switch channel 1
5	INB1	Input terminal of input selector switch channel 1
6	INC1	Input terminal of input selector switch channel 1
7	IND1	Input terminal of input selector switch channel 1
8	DEFN OUT1	Differential output terminal (-)
9	SEL OUT1	Input selector output terminal
10	VOL IN1	Volume 1 input terminal
11	TONE OUT1	Tone output terminal
12	FADER IN1	Volume 2 input terminal
13	REAR OUT1	Fader volume control (Rear) output terminal
14	FRONT OUT1	Fader volume control (Front) output terminal
15	NonFader OUT1	Non fader volume output terminal
16	GND	GND terminal
17	DATA	Control data input terminal
18	VDDOUT1	Test terminal
19	VDDOUT2	Test terminal
20	CLOCK	Clock input terminal for serial data transport
21	VDD	Power supply terminal for digital
22	NonFader OUT2	Non fader volume control output terminal
23	FRONT OUT2	Fader volume (Front) output terminal
24	REAR OUT2	Fader volume (Rear) output terminal
25	FADER IN2	Volume 2 input terminal
26	TONE OUT2	Tone output terminal
27	VOL IN2	Volume 1 input terminal
28	SEL OUT2	Input selector output terminal
29	DEFN OUT1	Differential output terminal (-)
30	IND2	Input terminal of input selector switch channel 2
31	INC2	Input terminal of input selector switch channel 2
32	INB2	Input terminal of input selector switch channel 2
33	INA2	Input terminal of input selector switch channel 2
34	DEFN IN1	Differential motion amp negative input terminal
35	DEFP IN1	Differential motion amp positive input terminal
36	VCC	Power supply terminal

■ PCM1716E-X (IC802) : D/A converter

1. Pin layout



2. Block diagram

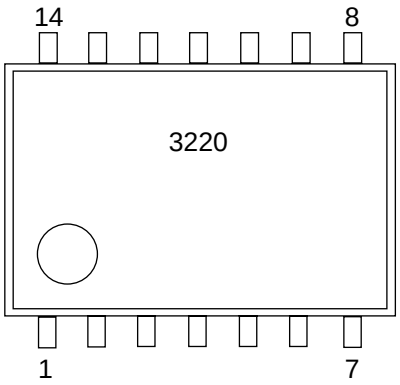


3. Pin function

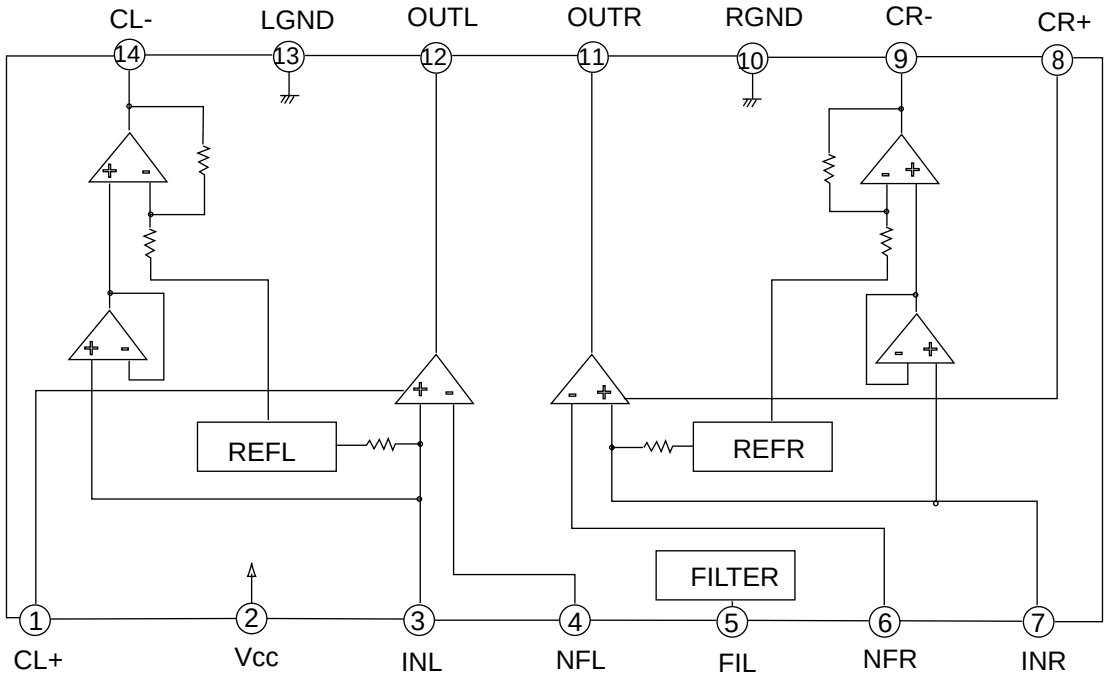
Pin No.	Symbol	I/O	Function
1	LRCK	I	LRCK clock input
2	DATA	I	Serial audio data input
3	BCK	I	Bit clock input for serial audio data
4	CLKO	O	Buffered output of system clock
5	XTI	I	Oscillator input / External clock input
6	XTO	O	Oscillator output
7	DGND	-	Digital ground
8	VDD	-	Digital power +5V
9	VDD2R	-	Analog power +5V
10	AGND2R	-	Analog ground
11	EXTR	O	Rch common pin of analog output amp
12	NC	-	Non connection
13	VOUTR	O	Rch analog voltage output of audio signal
14	AGND1	-	Analog ground
15	Vcc1	-	Analog power +5V
16	VOUTL	O	Lch analog voltage output of audio signal
17	NC	-	Non connection
18	EXTL	O	Lch common pin of analog output amp
19	AGND2L	-	Analog ground
20	Vcc2L	-	Analog power +5V
21	ZERO	O	Zero data flag
22	RST	I	Reset
23	CS/IWO	I	Chip select / Input format selection
24	MODE	I	Mode control select
25	MUTE	I	Mute control
26	MD/DM0	I	Mode control, Data / De-emphasis selection 1
27	MC/DM1	I	Mode control, BCK / De-emphasis selection 2
28	ML/IIS	I	Mode control, WDCK / Input format selection

■ BA3220FV-X (IC301,IC401) : Line out amp

1.Pin layout

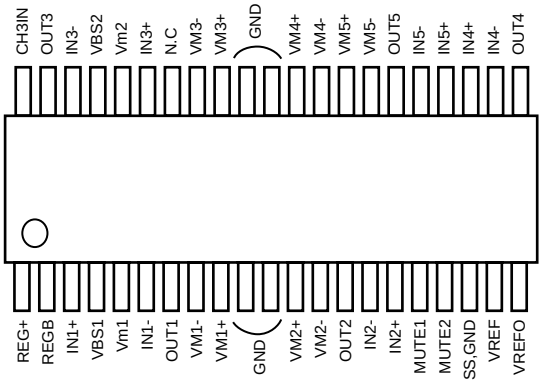


2.Block diagram

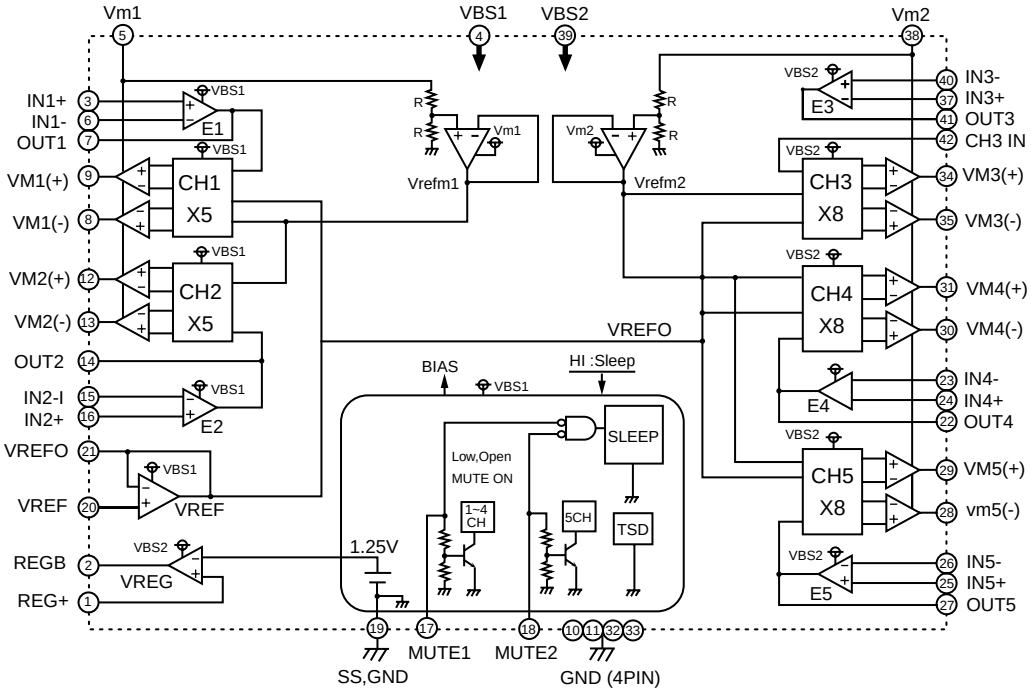


■ M63008FP-X (IC604) : 5ch Actuator driver

1.Pin layout

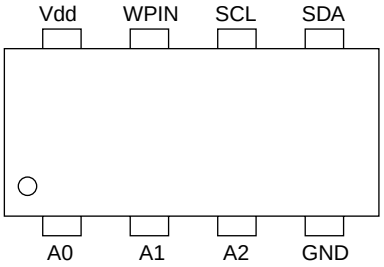


2.Block diagram



■ BR24C16F-X (IC703) : EEPROM

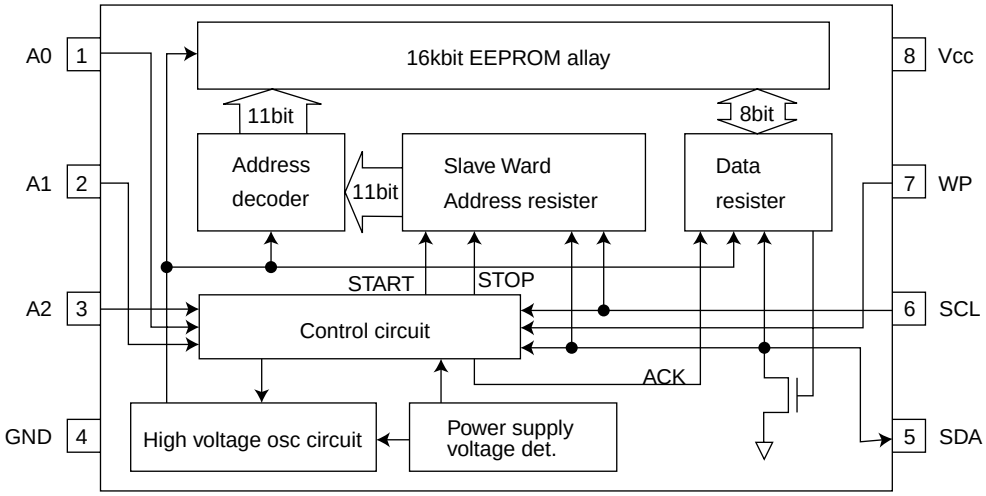
1. Pin layout



2. Pin function

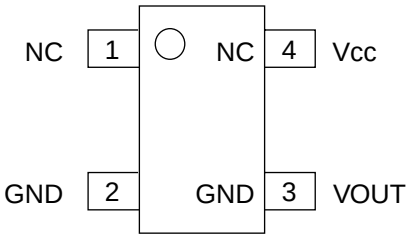
Symbol	I/O	Function
Vdd	-	Power supply.
GND	-	GND
A0,A1,A2	I	No use connect to GND.
SCL	I	Serial clock input.
SDA	I/O	Serial data I/O of slave and ward address.
WPIN	I	Write protect terminal.

3. Block diagram

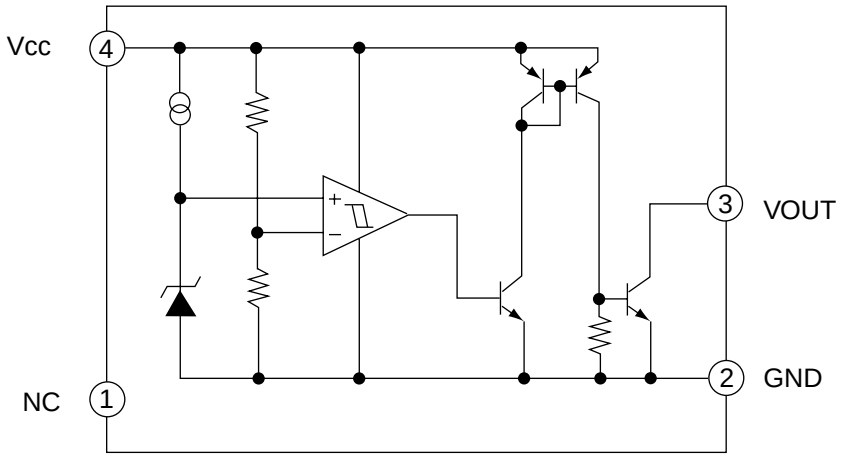


■ IC-PST9333U-X (IC702) : Reset IC

1. Pin layout



2. Block diagram

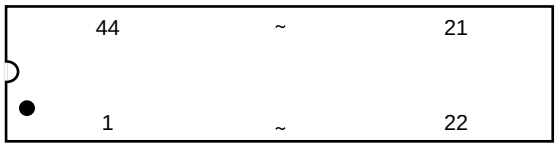


3. Pin function

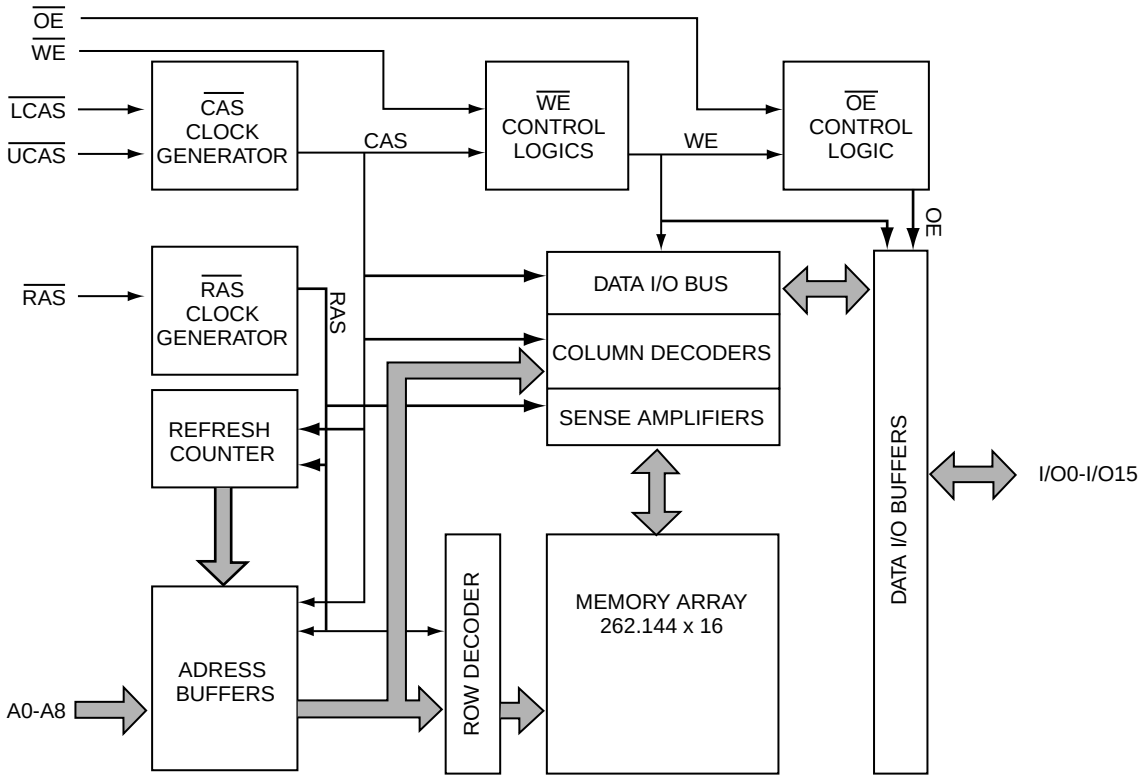
Pin No.	Symbol	Function
1	NC	Non connect
2	GND	GND terminal
3	VOUT	Reset signal output terminal
4	Vcc	Power supply terminal

■IS41C16256-35T(IC602):RAM

1.Pin layout

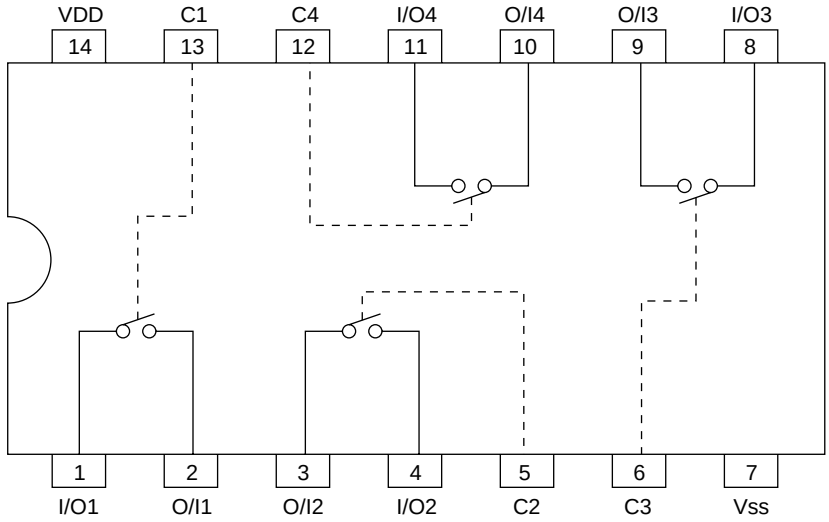


2.Block diagram



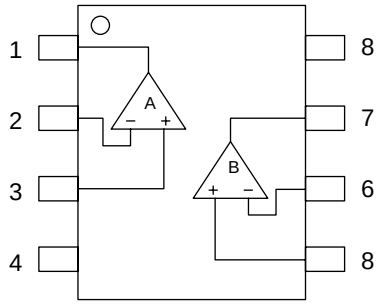
■BU4066BCFV-X (IC322) : Quad analog switch

1. Pin layout & Block diagram



■ NJM4565V-X (IC171,IC951,IC323) : Ope amp

1. Pin layout & Block diagram

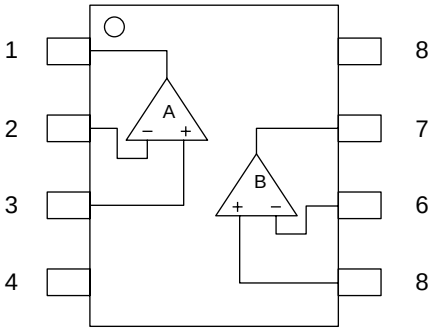


2. Pin function

Pin No.	Function
1	A output
2	A-input
3	A+input
4	V-
5	B+input
6	B-input
7	B output
8	V+

■ NJM4580V-X (IC801) : CD LPF

1. Pin layout & Block diagram

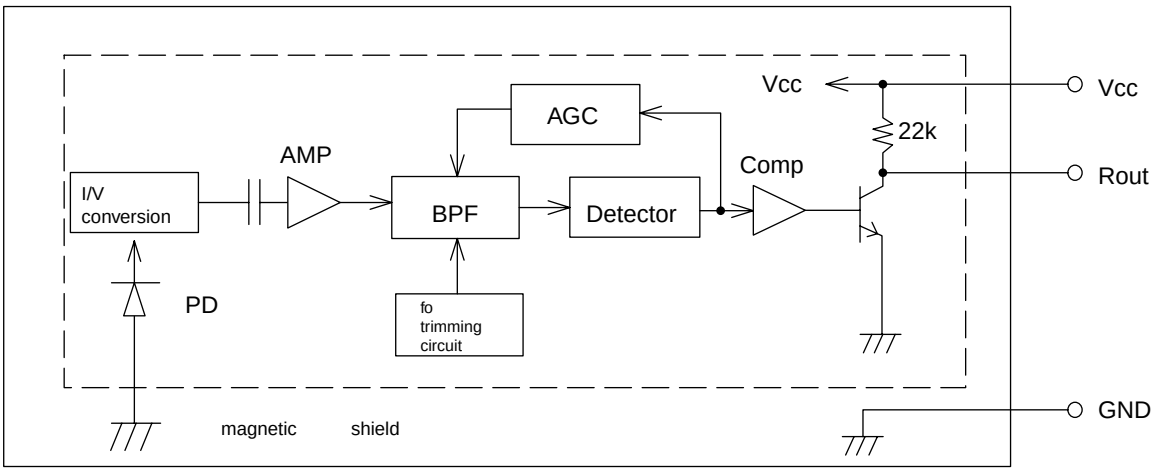


2. Pin function

Pin No.	Function
1	A output
2	A -input
3	A +input
4	V-
5	B +input
6	B -input
7	B output
8	V+

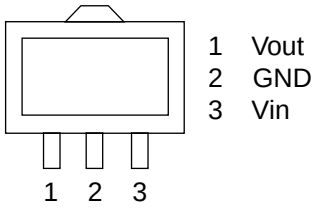
■ RPM6938-SV4 (IC561) : Remote sensor

1.Block diagram

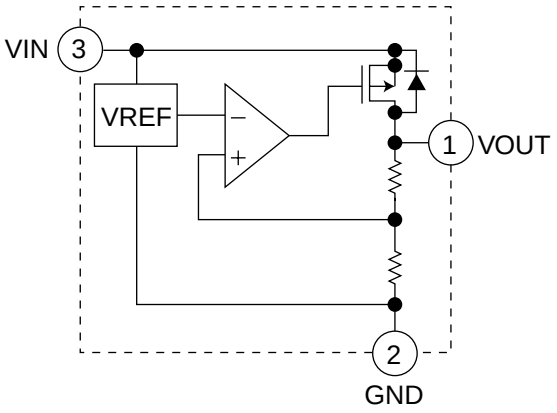


■ S-81332HG-KC-X (IC804) : Regulator

1. Pin layout

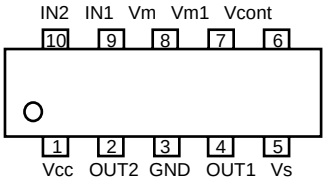


2. Block diagram

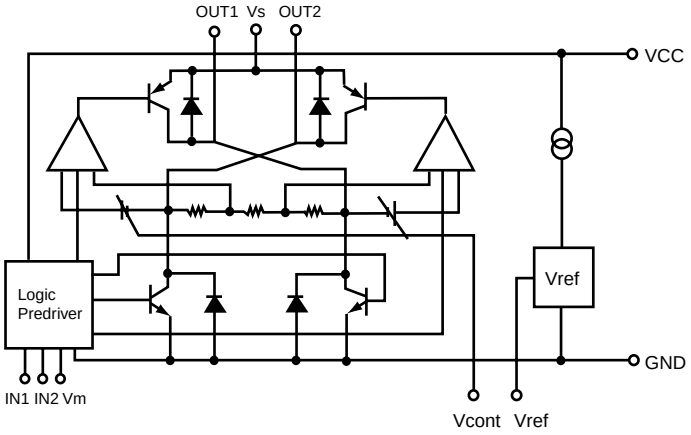


■ LB1830M-X(IC608):Regulator

1.Pin layout

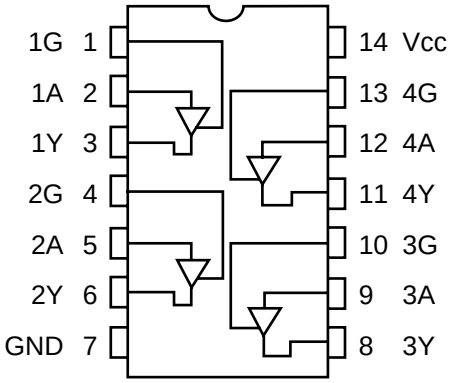


2.Block diagram



■ TC74VHC126FT-X(IC605):Buffer

1.Pin layout



2.Function

INPUTS		OUTPUT
G	A	Y
L	X	Z
H	L	L
H	H	H

X:Don't Care
Z: High impedance

JVC

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